(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 December 2007 (21.12.2007)

PCT

(10) International Publication Number
WO 2007/145701 A2

(51) International Patent Classification: Not classified

(21) International Application Number:
PCT/US2007/008540

(22) International Filing Date: 6 April 2007 (06.04.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/790,322 7 April 2006 (07.04.2006) US

(71) Applicant *(for all designated States except US)*: **PRESIDENT AND FELLOWS OF HARVARD COLLEGE** [US/US]; 17 Quincy Street, Cambridge, MA 02138 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **NAM, Sung, Woo** [KR/US]; 35 Oxford Street, Perkins Hall, #416, Cambridge, MA 02138 (US). **JAVEY, Ali** [US/US]; 10 Fernald Drive, #23, Cambridge, MA 02138 (US). **LIEBER, Charles, M.** [US/US]; 27 Hayes Avenue, Lexington, MA 02137 (US).

(74) Agent: **OYER, Timothy, J.**; Wolf, Greenfield & Sacks, P.c., 600 Atlantic Avenue, Boston, MA 02210 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

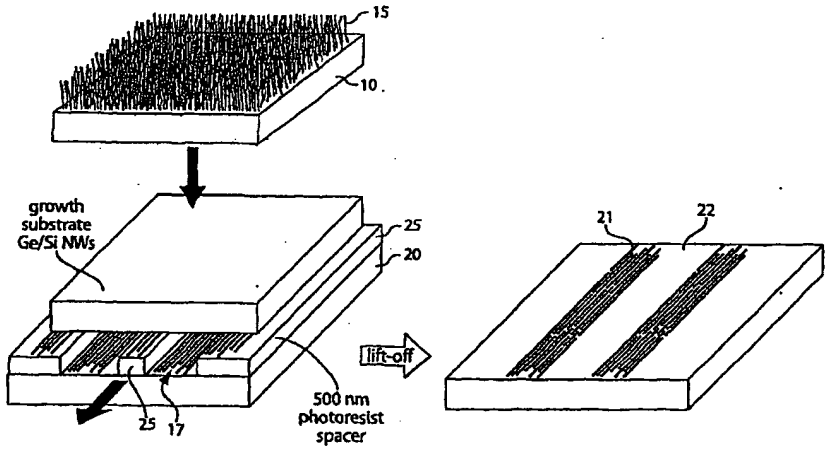
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: NANOSCALE WIRE METHODS AND DEVICES



(57) Abstract: The present invention generally relates to nanoscale wire methods and devices, including systems and methods for positioning nanoscale wires on a surface, and articles made therefrom. One aspect of the invention is generally directed to aligned nanoscale wires on a surface of a substrate, and systems and methods of positioning such nanoscale wires on the surface. In one set of embodiments, a first substrate is provided having a plurality of nanoscale wires, and at least some of the nanoscale wires are transferred to a second substrate by contacting at least some of the nanoscale wires with the second substrate, e.g., by moving or "sliding" the substrates relative to each other, in some cases causing alignment of the nanoscale wires on the second substrate. Another aspect of the invention is generally directed to electrical devices comprising a number of planes defined by nanoscale wires, e.g., in a "stacked" configuration. Yet other aspects of the invention are directed to nanoscale wires that can be used as sensors, e.g., in such devices. Still other aspects of the invention are directed to systems and methods for making and using such devices, kits involving the same, and the like.

WO 2007/145701 A2

NANOSCALE WIRE METHODS AND DEVICES

RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Patent Application Serial No. 60/790,322, filed April 7, 2006, entitled "Nanoscale Wire Methods and Devices," by Lieber, *et al.*, incorporated herein by reference.

FIELD OF INVENTION

The present invention generally relates to nanoscale wire methods and devices, including systems and methods for positioning nanoscale wires on a surface, and articles made therefrom.

BACKGROUND

Interest in nanotechnology, in particular sub-microelectronic technologies such as semiconductor quantum dots and nanoscale wires, has been motivated by the challenges of chemistry and physics at the nanoscale, and by the prospect of utilizing these structures in electronic and related devices. Nanoscopic articles might be well-suited for transport of charge carriers and excitons (e.g. electrons, electron pairs, etc.) and thus may be useful as building blocks in nanoscale electronics applications. Nanoscale wires are well-suited for efficient transport of charge carriers and excitons, and thus are expected to be important building blocks for nanoscale electronics and optoelectronics.

SUMMARY OF THE INVENTION

The present invention generally relates to nanoscale wire methods and devices, including systems and methods for positioning nanoscale wires on a surface, and articles made therefrom. The subject matter of the present invention involves, in some cases, interrelated products, alternative solutions to a particular problem, and/or a plurality of different uses of one or more systems and/or articles.

In one aspect, a method is provided. In one set of embodiments, the method includes acts of providing a first substrate having a plurality of nanoscale wires thereon, contacting at least some of the plurality of nanoscale wires with a second substrate, and transferring at least some of the plurality of nanoscale wires from the first substrate to the second substrate.

The method, according to another set of embodiments, includes acts of providing a first substrate having a plurality of nanoscale wires attached to a surface of the

substrate via respective points of attachment, contacting at least some of the plurality of nanoscale wires with a second substrate, and moving at least one of the first and second substrates such that at least some of the plurality of nanoscale wires are moved into an orientation substantially parallel to the surface of the first substrate.

In yet another set of embodiments, the method includes acts of providing a substrate having a plurality of nanoscale wires attached to a surface of the substrate via respective points of attachment, and applying a force to at least some of the plurality of nanoscale wires such that at least some of the plurality of nanoscale wires are moved into an orientation substantially parallel to the surface of the substrate.

The method, according to still another set of embodiments, includes acts of providing a substrate having a plurality of nanoscale wires attached to a surface of the substrate via respective points of attachment, and rotating at least some of the plurality of nanoscale wires substantially around the respective points of attachment.

In still another set of embodiments, the method includes acts of providing a first substrate having a plurality of nanoscale wires attached to a surface of the first substrate via respective points of attachment, providing a second substrate spaced a distance away from the first substrate, the second substrate substantially parallel to the first substrate, such that at least one nanoscale wire attached to the first substrate is in physical contact with the second substrate, and decreasing the spacing between the first substrate and the second substrate such that the first substrate and the second substrate remain substantially parallel.

Yet another set of embodiments provides an act of aligning a plurality of nanoscale wires substantially parallel relative each other on a surface of a substrate without exposing the plurality of nanoscale wires to a liquid.

Still another set of embodiments is directed to a method of providing a substrate comprising a first layer of nanoscale wires, depositing an intermediate layer of non-fluid material on the first layer of nanoscale wires, and depositing a second layer of nanoscale wires on the intermediate layer of non-fluid material.

In one set of embodiments, the article includes a unitary device comprising at least 5 planar layers of circuitry. In another set of embodiments, the article includes a functioning device comprising at least 3 planar layers. In some cases, the device ceases to function at a temperature of at least about 500 °C.

An article is contemplated in another aspect of the invention. In one set of embodiments, the article includes a first substrate, a second substrate substantially parallel to the first substrate, and a plurality of nanoscale wires. In some cases, at least some of the nanoscale wires each has a first end in contact with the first substrate and a second end in contact with the second substrate not immobilized relative to the first substrate.

The article, in another set of embodiments, includes a substrate having a surface, and a plurality of nanoscale wires each having an end in contact with the surface of the substrate. In some instances, substantially all of the plurality of nanoscale wires are not substantially perpendicular to, and are not substantially parallel with, the surface of the substrate.

In yet another set of embodiments, the article includes a first plurality of nanoscale wires intersected by a first plane, a second plurality of nanoscale wires intersected by a second plane, and an intermediate layer of non-fluid material positioned between the first plane of nanoscale wires and the second plane of nanoscale wires.

According to another set of embodiments, the method includes acts of providing a substrate comprising a first layer of nanoscale wires, at least some of which are substantially parallel, and depositing, with respect to the substrate, a second layer of nanoscale wires, at least some of which are substantially parallel to the first substantially parallel nanoscale wires.

In one set of embodiments, the method includes an act of forming an electronic circuit comprising nanoscale wires, substantially aligned in parallel relative to each other, disposed on a photoresist.

In another aspect, the present invention is directed to a method of making one or more of the embodiments described herein, for example, a plurality of aligned nanoscale wires on a surface of a substrate. In another aspect, the present invention is directed to a method of using one or more of the embodiments described herein.

Other advantages and novel features of the present invention will become apparent from the following detailed description of various non-limiting embodiments of the invention when considered in conjunction with the accompanying figures. In cases where the present specification and a document incorporated by reference include conflicting and/or inconsistent disclosure, the present specification shall control. If t

or more documents incorporated by reference include conflicting and/or inconsistent disclosure with respect to each other, then the document having the later effective date shall control.

BRIEF DESCRIPTION OF THE DRAWINGS

Non-limiting embodiments of the present invention will be described by way of example with reference to the accompanying figures, which are schematic and are not intended to be drawn to scale. In the figures, each identical or nearly identical component illustrated is typically represented by a single numeral. For purposes of clarity, not every component is labeled in every figure, nor is every component of each embodiment of the invention shown where illustration is not necessary to allow those of ordinary skill in the art to understand the invention. In the figures:

Figs. 1A-1B are examples of schematic illustrations of certain processes of the invention;

Fig. 2 illustrates a method of producing aligned nanoscale wires on the surface of a substrate, according to one embodiment of the invention;

Figs. 3A-3B are photomicrographs of aligned nanowires on a substrate, in another embodiment of the invention;

Figs. 4A-4B illustrate thin film transistors produced using an embodiment of the invention;

Figs. 5A-5B illustrate variations in transistor characteristics produced in one embodiment of the invention;

Fig. 6A-6C illustrate the fabrication of a multi-layer device according to another embodiment of the invention;

Fig. 7 is a photomicrograph of a 10-layer device, produced according to one embodiment of the invention;

Fig. 8 is a graph illustrating that the addition of a layer of material on top of an electrical component comprising nanoscale wires did not substantially alter the performance of the electrical component, in one embodiment of the invention;

Figs. 9A-9B illustrate that similar electrical components comprising nanoscale wires in different layers of a multi-layer device displayed similar characteristics, according to another embodiment of the invention;

Figs. 10A-10B illustrate performance of an inverter comprising nanoscale wires in one embodiment of the invention;

Figs. 11A-11C illustrate single-nanowire FETs, in yet another embodiment of the invention;

Figs. 12A-12D illustrate multifunctional circuits on plastics, in still another embodiment of the invention;

Figs. 13A-13B illustrate floating gate memory according to one embodiment of the invention;

Figs. 14A-14B illustrate interconnected PMOS FETs, in another embodiment of the invention;

Figs. 15A-15D illustrate a two layer PMOS nanowire inverter, according to yet another embodiment of the invention;

Figs. 16A-16F illustrate a two layer PMOS nanowire ring oscillator, according to still another embodiment of the invention;

Figs. 17A-17E illustrate a two layer CMOS nanowire ring oscillator, according to yet another embodiment of the invention; and

Figs. 18A-18D illustrate a two layer CMOS nanowire ring oscillator, according to still another embodiment of the invention.

DETAILED DESCRIPTION

The present invention generally relates to nanoscale wire methods and devices, including systems and methods for positioning nanoscale wires on a surface, and articles made therefrom. One aspect of the invention is generally directed to aligned nanoscale wires on a surface of a substrate, and systems and methods of positioning such nanoscale wires on the surface. In one set of embodiments, a first substrate is provided having a plurality of nanoscale wires, and at least some of the nanoscale wires are transferred to a second substrate by contacting at least some of the nanoscale wires with the second substrate, e.g., by moving or "sliding" the substrates relative to each other, in some cases causing alignment of the nanoscale wires on the second substrate. Another aspect of the invention is generally directed to electrical devices comprising a number of planes defined by nanoscale wires, e.g., in a "stacked" configuration. Yet other aspects of the invention are directed to nanoscale wires that can be used as sensors, e.g., in such

devices. Still other aspects of the invention are directed to systems and methods for making and using such devices, kits involving the same, and the like.

Embodiments

One aspect of the invention is generally directed to transferring nanoscale wires from a first substrate to a second substrate. In one set of embodiments, a first substrate or other article, having a plurality of nanoscale wires thereon, is brought into contact with a second article to transfer one or more nanoscale wires from one to the other. In one embodiment, the first article or substrate is moved or slid against a second substrate (and/or the second substrate is moved against the first substrate) such that at least some of the nanoscale wires are transferred from the first substrate to the second substrate. The nanoscale wires can become immobilized relative to the second substrate through ionic interactions, hydrophobic interactions, van der Waals interactions, etc., or the like.

The nanoscale wires may be nanowires, nanotubes, or the like, or any combination thereof. A nanowire is typically a solid wire (for example, a semiconductor nanowire), while a nanotube is typically hollow (for example, a carbon nanotube), or has a hollowed-out core. Nanoscale wires, nanowires, nanotubes, etc., are discussed in more detail below (see "Definitions"), including sizes and compositions, as well as techniques for fabricating such nanoscale wires. A nanoscale wire is typically straight, although in some cases, the nanoscale wire can be branched or curved. In some cases, the nanoscale wires may be rigid. If multiple nanoscale wires are present, the nanoscale wires may each independently have the same or different lengths, and/or the same or different diameters. In addition, the nanoscale wires may each independently have the same or different compositions. Non-limiting examples of nanoscale wires are discussed in detail below:

The nanoscale wires may be attached to the first substrate in any orientation, and by any suitable method. In some embodiments, the nanoscale wires are attached to the substrate at a single point of attachment, for example, such that the nanoscale wires are substantially perpendicular to the substrate. In other embodiments, however, the nanoscale wires can be attached to the substrate at a substantially non-perpendicular angle. In still other embodiments, a portion of the nanoscale wires may be in contact with the substrate, e.g., the nanoscale wire may be on its side with respect to the

substrate. In yet other embodiments, a plurality of nanoscale wires on a substrate may each independently exhibit some or all of these orientations.

In some embodiments, a first substrate may be used to grow some or all of the nanoscale wires, i.e., the first substrate is a growth substrate. The growth substrate may be formed from any material suitable for growing nanoscale wires therefrom. For example, the growth substrate can comprise silicon and/or other semiconductor materials. Techniques for growing nanoscale wires from a surface are known by those of ordinary skill in the art. For example, in one embodiment, particles such as gold particles and/or other particles (which particles may have the same or different sizes) are deposited on a growth substrate, e.g., using photolithography or other suitable techniques, and the particles are then used to nucleate and grow nanoscale wires from the surface of the substrate. As another example, vertically-oriented nanoscale wires may be etched from a semiconductor material by selectively removing portions of the semiconductor material to leave behind nanoscale wires attached to a substrate. Additional non-limiting examples of techniques for growing nanoscale wires on a surface are known to those of ordinary skill in the art, and are disclosed in more detail in W. Lu, *et al.*, "One-dimensional Hole Gas in Germanium/Silicon Nanowire Heterostructures," *Proc. Natl. Acad. Sci. USA*, 102, 10046-10051 (2005); L.J. Lauhon, *et al.*, "Epitaxial Core-Shell and Core-Multi-Shell Nanowire Heterostructures," *Nature*, 420, 57-61 (2002); as well as U.S. Pat. No. 5,858,862, issued January 12, 1999.

The nanoscale wires may be present on the substrate at any suitable density, and the density can be controlled using routine techniques, for instance, by controlling the deposition of particles onto the surface of the substrate. As an example, the density of nanoscale wires on a substrate may be at least about 1 nanoscale wires/micrometer^2, and in some cases, at least about 3, at least about 10, at least about 30, at least about 100, at least about 300, at least about 1,000, at least about 3,000, or at least about 10,000 nanoscale wires/micrometer^2, depending on the conditions used. Accordingly, very high densities of aligned nanoscale wires on a surface of a substrate can result when techniques such as those discussed below are used to pattern the nanowires onto a surface (see Figs. 3A and 3B for examples).

The nanoscale wires can then be transferred to a second substrate. In some cases the second substrate is a semiconductor material. However, in other cases, the second

substrate may be any other suitable material, for example, glass, a polymer, etc. As high temperatures are not necessary to transfer the nanoscale wires from the first substrate to the second substrate, the transfer may occur at any suitable temperature (including room temperature, 25 °C), and accordingly, the second substrate need not be able to withstand high temperatures. For example, the second substrate may begin to degrade at relatively high temperatures, e.g., such that it melts or decomposes, or such that the nanoscale wires are unable to remain attached to the nanoscale wire. Such degradation may occur, for instance, at temperatures greater than about 100 °C, greater than about 200 °C, greater than about 300 °C, greater than about 500 °C, greater than about 750 °C, greater than about 1000 °C, etc. Of course, in other embodiments, the second substrate is able to withstand relatively high temperatures. The choice of materials for the second substrate thus depends on the particular application.

In some embodiments, the second substrate may have a predetermined pattern of material thereon, e.g., for use in circuit fabrication. In some cases, the material may be used to prevent the two substrates from coming into full direct physical contact with each other, which may crush the nanoscale wires. For example, referring now to Fig. 2, where the first substrate comes into contact with the material, the nanoscale wires there may be crushed, but where the first substrate does not come into contact with the material (e.g., in the "valleys"), the nanoscale wires may not be crushed and can be subsequently used. The material may have any suitable height, for example, at least about 10 nm, at least about 30 nm, at least about 100 nm, at least about 200 nm, at least about 300 nm, at least about 500 nm, at least about 750 nm, at least about 1 micrometer, etc.

Thus, the second substrate may be non-flat, but contain different levels of materials that can prevent the two substrates from coming into full direct physical contact with each other. As mentioned, the second substrate may be flat but contain predetermined pattern of material thereon, and/or the second substrate may be non-flat (i.e., the second substrate itself may contain different levels of materials) to prevent full direct physical contact. For instance, the second substrate may have a series of "ridges," "valleys," stops, posts, pillars, protrusions, or the like, at any suitable height (relative to their bases), e.g., at least about 10 nm, at least about 30 nm, at least about 100 nm, at least about 200 nm, at least about 300 nm, at least about 500 nm, at least about 750 nm, at least about 1 micrometer, etc.

As another example, the second substrate may comprise one or more materials that are removed from the second substrate during fabrication of the circuit, and/or the second substrate may comprise materials, such as electrodes, interconnects (e.g., copper, aluminum, gold, silver, etc.), dielectric materials, insulators, other electrical components, etc., for use in the finished circuit. As non-limiting examples, materials that can be removed from the second substrate during fabrication include photoresist such as SU-8, Novolac, or diazonaphthoquinone

The second substrate, in certain embodiments, may contain one or more regions that are free of additional materials deposited thereon, and one or more regions containing additional materials as described above. Techniques for depositing the additional materials onto a substrate are well-known to those of ordinary skill in the art, and those of ordinary skill in the art will be able to design and fabricate suitable circuits using such materials and techniques. Nanoscale wires that are transferred from the first substrate may be transferred to one or both of these regions. As mentioned, in some instances, the additional material (or portions thereof) may then be subsequently removed, e.g., during the fabrication process, as discussed below, which also removes the nanoscale wires transferred to those portions.

The second substrate may be contacted with the nanoscale wires attached to the first substrate. If the nanoscale wires attached to the first substrate are attached via a point of attachment (i.e., the nanoscale wires are perpendicular and/or at an angle relative to the first substrate), the second substrate can contact the nanoscale wires without necessarily coming into direct physical contact with the first substrate. In some cases, the second substrate can thus be moved into a position such that at least some of the nanoscale wires each have a first end in contact with the first substrate and a second end in contact with the second substrate. In some cases, the second substrate is provided at a spacing away from the first substrate (e.g., parallel to the first substrate), then brought into contact with the first substrate and/or with the nanoscale wires attached to the first substrate. The two substrates can be positioned in any suitable orientation. For example, the first substrate (having the nanoscale wires) may be inverted and held above the second substrate (Fig. 1B), or the second substrate may be held above the first substrate (Fig. 1A).

In some embodiments, the two substrates are moved or slid relative to each other such that at least some of the nanoscale wires are moved into an orientation substantially parallel to the surface of the first substrate, i.e., the second substrate may be used to force the nanoscale wires to "flatten," e.g., from a substantially perpendicular orientation to a diagonal (i.e., non-perpendicular and non-parallel) orientation or even an orientation substantially parallel to the surface of the first substrate. The nanoscale wires may thus become aligned during this operation, i.e., oriented in substantially the same direction. The spacing between the two substrates may also be reduced during this operation such that the spacing is less than the average length of the nanoscale wires, e.g., less than half the average length of the nanoscale wires, or even closer, which may cause the nanowires to flatten. This technique may be performed using any suitable method, e.g., manually or mechanically.

Of course, in other embodiments, other forces can be used to force the nanoscale wires from a substantially perpendicular orientation to a diagonal orientation or a substantially parallel orientation. For example, a force could be applied to the nanoscale wires via a fluid, or an electrical or magnetic force may be used. Application of a force on the nanoscale wires may cause at least some of the nanoscale wires to rotate substantially around their respective points of attachment.

An example of a schematic illustration of this process is shown in Fig. 1A. In this figure, first substrate 10, containing nanoscale wires 15, is brought towards second substrate 20. The two substrates 10 and 20 are held parallel, such that at least some of nanoscale wires 15 contact substrate 20. The two substrates 10 and 20 are then slid relative to each other and towards each other, which causes nanoscale wires 15 to "flatten" or rotate to a substantially parallel orientation. The second substrate 20 is then removed, leaving flatten nanoscale wires 15 on the surface of first substrate 10.

The nanoscale wires (or at least a portion thereof) may also be transferred from the first substrate to the second substrate. In some cases, the nanoscale wires are attracted to the second substrate. In other cases, transfer of the nanoscale wires may be effected by "moving" or "sliding" one of the substrates in a direction substantially parallel to a surface of the other substrate, i.e., the two substrates are moved or slid relative to the other. The spacing between the two substrates may also be reduced in some cases during this operation such that the spacing is less than the average length of

the nanoscale wires, e.g., less than half the average length of the nanoscale wires, or even closer, which may force the nanoscale wires to "flatten," facilitating transfer of the nanoscale wires. As mentioned, this may be performed using any suitable method, e.g., manually or mechanically. In some cases, sliding the substrates in such a fashion is able to cause at least some of the plurality of nanoscale wires to be transferred from the first substrate to the second substrate. Due to the relative movements of the two substrates, some of the nanoscale wires may become aligned on the second substrate. In some cases, the first substrate and the second substrate are held substantially parallel during the transfer. Afterwards, in some cases, the first substrate can be removed.

An example of a schematic illustration of this process is shown in Fig. 1B. Here, first substrate 10, containing nanoscale wires 15, is inverted and brought towards second substrate 20. The two substrates 10 and 20 are held parallel, such that at least some of nanoscale wires 15 contact substrate 20. The two substrates 10 and 20 are then slid relative to each other and towards each other, which causes nanoscale wires 15 to "flatten" or rotate to a substantially parallel orientation. While in contact, at least some of nanoscale wires 15 become immobilized relative to second substrate 20, for instance, through ionic interactions, hydrophobic interactions, van der Waals interactions, etc., or the like. The first substrate 10 is then removed, leaving behind substantially oriented nanoscale wires 15 on the surface of substrate 20.

Accordingly, in certain embodiments of the invention, a plurality of nanoscale wires can be deposited onto the surface of a substrate without exposing the plurality of nanoscale wires to a liquid and/or to a surfactant, in contrast with other methods of nanoscale wire alignment that require exposure of the nanoscale wires to a liquid and/or to a surfactant (which may leave behind residual surfactant after exposure). In addition, such deposition may occur at any suitable temperature, including at room temperature. Such nanoscale wires can be used in any suitable electronic device or component, as discussed herein.

In some cases, as mentioned, the second substrate may have a predetermined pattern of material thereon. Some of the nanoscale wires transferred from the first substrate to the second substrate may be deposited on this material, instead of on the second substrate itself. In some cases, some of this material may be removed, for example, a photoresist material may be etched away from the second substrate using

techniques known to those of ordinary skill in the art. Typically, this process also causes removal of any nanoscale wires positioned thereon. Thus, by selective removal of the photoresist or other materials, nanoscale wires may be removed from certain regions of the second substrate without removing the nanoscale wires from other regions of the second substrate. Accordingly, nanoscale wires can be deposited into specific, predetermined regions of the second substrate, e.g., for use in circuit or component fabrication. An example can be seen in Fig. 4A, which shows regions ("channels") containing germanium/silicon nanowires, and regions free of nanowires.

In some embodiments, additional material may be deposited onto the nanoscale wires. For example, additional nanoscale wires may be deposited onto the nanoscale wires (e.g., using the above-described techniques, in the same or in different orientations as the first layer of nanoscale wires), and/or other materials may be deposited onto the nanoscale wires, for example, electrodes, interconnects (e.g., copper, aluminum, gold, silver, etc.), dielectric materials, insulators, other electrical components, or the like, e.g., such that the nanoscale wires can be used as part of an electric circuit, and/or as a component for an electric circuit. Non-limiting examples of components that can be produced using such processes include transistors (e.g., thin film transistors) and invertors, which are discussed below in the examples. Other non-limiting examples include switches, diodes, LEDs, sensors, logic gates, latches, rectifiers, memory, transistors such as FET (field effect transistors), inverters, ring oscillators, or the like.

In some cases, an additional layer of material may be deposited on the nanoscale wires. The material may be solid, or another non-fluid material; e.g., a gel. The additional layer of material may be insulating in some cases, e.g., comprising photoresist. In some cases, the additional layer of material may be deposited without heating the material to relatively high temperatures, such as greater than about 500 °C, greater than about 750 °C, greater than about 1000 °C, etc. The additional layer of material may serve as a new second substrate in certain instances, e.g., for the deposition of a new layer of nanoscale wires thereon, such as aligned nanoscale wires, as previously described.

By repeating the above-described techniques as desired, an electronic device having more than one layer or plane of nanoscale wires may be produced, and thus, another aspect of the invention is directed to a device comprising a plurality of layers of

nanoscale wires. In some cases, the device is unitary. "Unitary," as used herein, means a device which is not readily disassembled into components, e.g., it can be a solid structure which would need to be broken or otherwise disassembled outside of its ordinary use to be divided into components. In this arrangement, the unitary device can include only the particular layers of nanoscale wires described below, or the unitary nature of the device can extend to other parts of an overall device or component. The device can have any number of layers of nanoscale wires (for instance, the device may have 2, 3, 4, 5, 6, 7, 8, 9, or 10 layers of nanoscale wires) and any number of intermediate layers of materials. Additionally, other materials or components may be present within the device as well, for example, circuitry without any nanoscale wires present, electrodes, interconnects (e.g., copper, aluminum, gold, silver, etc.), dielectric materials, insulators, etc.

Typically, the layers are substantially parallel. In some cases, one or more of the layers of nanoscale wires (or other layers comprising circuitry) may be electrical communication; however, it is not required that all of the layers of the device be in electrical communication. Also, as mentioned above, in some cases, there may be more than one layer of nanoscale wires in physical contact (i.e., without an intermediate layer of material present between the two layers of nanowires).

In some cases, one or more of the layers of nanoscale wires may comprise aligned nanoscale wires (e.g., produced as previously described), and in certain embodiments, if more than one layer is present comprising aligned nanoscale wires, the aligned nanoscale wires of any two or more of the layers may be substantially aligned in a common direction. In other cases, however, one or more of the layers of nanoscale wires may comprise nanoscale wires that are not aligned. In certain cases, a layer of nanoscale wires may comprise some nanoscale wires that are aligned and some that are not aligned.

Accordingly, by using techniques such as those described herein, a unitary device can be fabricated comprising any number of planar layers of circuitry, some layers of which may comprise nanoscale wires. The device may be prepared without the use of high temperatures in certain embodiments of the invention, e.g., temperatures greater than about 500 °C, greater than about 750 °C, greater than about 1000 °C, etc. Thus, in some cases, materials can be used within the device which degrade at relatively high

temperatures, e.g., certain types of polymers that can melt or degrade when exposed to relatively high temperatures. In some instances, such as when such materials are used, the device may cease to function at higher temperatures. Thus, in one set of embodiments, the unitary device may be fabricated on polymers such as Kapton, a polyimide, etc., e.g., which can be used as a substrate within the device. In some cases, the substrate may be chosen so as to be flexible. The unitary device may be used for any application. For instance, in one set of embodiments, the unitary device can be used as a memory storage device. For example, a floating gate memory can be constructed. An example of a technique for constructing such a device is shown in the examples, below. Other examples include transistors such as field effect transistors, inverters, ring oscillators, or the like, and may be PMOS- and/or CMOS-based.

Still another aspect of the invention is a sensor that comprises one or more nanoscale wires, and/or functionalized nanoscale wires (e.g., with a reaction entity immobilized relative thereto, as discussed below), either uniformly or non-uniformly. The nanoscale wires may be aligned and/or positioned on a surface and/or as part of an electronic circuit or a multi-layer device, such as previously described. In certain embodiments, functionalization of the nanoscale wires permit interaction of the nanoscale wire with various analytes, such as molecular entities, and the interaction induces a change in a property of the functionalized nanoscale wires, which provides a mechanism for a sensor device.

As mentioned, using the techniques including those described herein, a plurality of nanoscale wires can be deposited onto the surface of a substrate without exposing the plurality of nanoscale wires to a liquid and/or to a surfactant. In addition, such deposition may occur at any suitable temperature, including at room temperature or biologically relevant temperatures (e.g., 37 °C). Such conditions may be advantageous in some instances for sensor devices comprising nanoscale wires, as surfactants and/or relatively high temperatures may make it more difficult to fabricate such sensor devices comprising nanoscale wires, and/or such nanoscale wire sensor devices may have inferior characteristics due to the presence of surfactants and/or high temperatures during the fabrication process.

In some cases, the nanoscale wires are functionalized, i.e. the nanoscale wires comprise surface functional moieties, to which the analytes binds and induces a

measurable property change to the nanoscale wire. The binding events can be specific or non-specific. The functional moieties may include simple groups, selected from the groups including, but not limited to, –OH, -CHO, -COOH, $-SO_3H$, -CN, $-NH_2$, -SH, -COSH, COOR, halide; biomolecular entities including, but not limited to, amino acids, proteins, sugars, DNA, antibodies, antigens, and enzymes; grafted polymer chains with chain length less than the diameter of a nanoscale wire core, selected from a group of polymers including, but not limited to, polyamide, polyester, polyimide, polyacrylic; a thin coating covering the surface of the nanoscale wire core, including, but not limited to, the following groups of materials: metals, semiconductors, and insulators, which may be a metallic element, an oxide, an sulfide, a nitride, a selenide, a polymer, a polymer gel, etc. In certain cases, the nanoscale wires used in the sensor may be free of surfactant, as previously discussed. Surfactant-free nanowires may allow a higher degree of functionalization to occur. In some embodiments, the invention provides one or more nanoscale wires and a reaction entity with which the analyte interacts, positioned in relation to the nanoscale wires such that the analyte can be determined by determining a change in characteristics of the nanoscale wires.

Chemical changes associated with the nanoscale wires can be used in some embodiments to modulate the properties of the wires and create electronic devices of a variety of types. The presence of the analyte can change the electrical properties of the nanoscale wire through electrocoupling with a binding agent of the nanoscale wire. If desired, the nanoscale wires can be coated with a specific reaction entity, binding partner or specific binding partner, chosen for its chemical or biological specificity to a particular analyte.

The term "reaction entity" refers to any entity that can interact with an analyte in such a manner to cause a detectable change in a property of a nanoscale wire. The reaction entity may enhance the interaction between the nanoscale wire and the analyte, or generate a new chemical species that has a higher affinity to the nanoscale wire, or to enrich the analyte around the nanoscale wire. The reaction entity can comprise a binding partner to which the analyte binds. The reaction entity, when a binding partner, can comprise a specific binding partner of the analyte. For example, the reaction entity may be a nucleic acid, an antibody, a sugar, a carbohydrate or a protein. Alternatively, the reaction entity may be a polymer, catalyst, or a quantum dot. A reaction entity that is a

catalyst can catalyze a reaction involving the analyte, resulting in a product that causes a detectable change in the nanoscale wire, e.g. via binding to an auxiliary binding partner of the product electrically coupled to the nanoscale wire. Another exemplary reaction entity is a reactant that reacts with the analyte, producing a product that can cause a detectable change in the nanoscale wire. The reaction entity can comprise a coating on the nanoscale wire, e.g. a coating of a polymer that recognizes molecules in, e.g., a gaseous sample, causing a change in conductivity of the polymer which, in turn, causes a detectable change in the nanoscale wire.

The term "binding partner" refers to a molecule that can undergo binding with a particular analyte, or "binding partner" thereof, and includes specific, semi-specific, and non-specific binding partners as known to those of ordinary skill in the art. For example, Protein A is usually regarded as a "non-specific" or semi-specific binder. The term "specifically binds," when referring to a binding partner (e.g., protein, nucleic acid, antibody, etc.), refers to a reaction that is determinative of the presence and/or identity of one or other member of the binding pair in a mixture of heterogeneous molecules (e.g., proteins and other biologics). Thus, for example, in the case of a receptor/ligand binding pair the ligand would specifically and/or preferentially select its receptor from a complex mixture of molecules, or vice versa. An enzyme would specifically bind to its substrate, a nucleic acid would specifically bind to its complement, an antibody would specifically bind to its antigen. Other examples include, nucleic acids that specifically bind (hybridize) to their complement, antibodies specifically bind to their antigen, and the like. The binding may be by one or more of a variety of mechanisms including, but not limited to ionic interactions, and/or covalent interactions, and/or hydrophobic interactions, and/or van der Waals interactions, etc.

The term "sample" refers to any cell, tissue; or fluid from a biological source (a "biological sample"), or any other medium, biological or non-biological, that can be evaluated in accordance with the invention including, such as serum or water. The sample may be contained in a fluid, e.g., in solution. A sample includes, but is not limited to, a biological sample drawn from an organism (e.g. a human, a non-human mammal, an invertebrate, a plant, a fungus, an algae, a bacteria, a virus, etc.), a sample drawn from food designed for human consumption, a sample including food designed for animal consumption such as livestock feed, milk, an organ donation sample, a sample of

blood destined for a blood supply, a sample from a water supply, or the like. One example of a sample is a sample drawn from a human or animal to determine the presence or absence of a specific nucleic acid sequence.

A "sample suspected of containing" a particular component means a sample with respect to which the content of the component is unknown. "Sample" in this context includes naturally-occurring samples, such as physiological samples from humans or other animals, samples from food, livestock feed, etc. Typical samples taken from humans or other animals include tissue biopsies, cells, whole blood, serum or other blood fractions, urine, ocular fluid, saliva, or fluid or other samples from tonsils, lymph nodes, needle biopsies, etc.

The term "electrically coupled" when used with reference to a nanoscale wire and an analyte, or other moiety such as a reaction entity, refers to an association between any of the analyte, other moiety, and the nanoscale wire such that electrons can move from one to the other, or in which a change in an electrical characteristic of one can be determined by the other. This can include electron flow between these entities, or a change in a state of charge, oxidation, or the like that can be determined by the nanoscale wire. As examples, electrical coupling can include direct covalent linkage between the analyte or other moiety and the nanoscale wire, indirect covalent coupling (e.g. via a linker), direct or indirect ionic bonding between the analyte (or other moiety) and the nanoscale wire, or other bonding (e.g. hydrophobic bonding). In some cases, no actual bonding may be required and the analyte or other moiety may simply be contacted with the nanoscale wire surface. There also need not necessarily be any contact between the nanoscale wire and the analyte or other moiety where the nanoscale wire is sufficiently close to the analyte to permit electron tunneling between the analyte and the nanoscale wire.

One embodiment of the invention involves a sensing element, which can be an electronic sensing element, and one or more nanoscale wires able to detect the presence, or absence, of an analyte in a sample (e.g. a fluid sample) containing, or suspected of containing, the analyte. In some cases, the sensing element may comprise a plurality of aligned nanoscale wires. Nanoscale sensors of the invention may be used, for example, in chemical applications to detect pH or the presence of metal ions; in biological applications to detect a protein, nucleic acid (e.g. DNA, RNA, etc.), a sugar or

carbohydrate, and /or metal ions; and in environmental applications to detect pH, metal ions, or other analytes of interest.

Another embodiment of the present invention provides an article comprising one or more nanoscale wires and a detector constructed and arranged to determine a change in an electrical property of the nanoscale wire. At least a portion of the nanoscale wires (which may be aligned in some cases) is addressable by a sample containing, or suspected of containing, an analyte. The phrase "addressable by a fluid" is defined as the ability of the fluid to be positioned relative to the nanoscale wire so that an analyte suspected of being in the fluid is able to interact with the nanoscale wire. The fluid may be proximate to or in contact with the nanoscale wire.

The criteria for selection of nanoscale wires and other conductors or semiconductors for use in the invention are based, in some instances, mainly upon whether the nanoscale wire itself is able to interact with an analyte, or whether the appropriate reaction entity, e.g. binding partner, can be easily attached to the surface of the nanoscale wire, or the appropriate reaction entity, e.g. binding partner, is near the surface of the nanoscale wire. Selection of suitable conductors or semiconductors, including nanoscale wires, will be apparent and readily reproducible by those of ordinary skill in the art with the benefit of the present disclosure.

The reaction entity may be positioned relative to the nanoscale wire to cause a detectable change in the nanoscale wire. The reaction entity may be positioned within 100 nanometers of the nanoscale wire, preferably with in 50 nanometers of the nanoscale wire, and more preferably with in 10 nanometers of the nanoscale wire, and the proximity can be determined by those of ordinary skill in the art. In one embodiment, the reaction entity is positioned less than 5 nanometers from the nanoscopic wire. In alternative embodiments, the reaction entity is positioned with 4 nm, 3 nm, 2 nm, and 1 nm of the nanoscale wire. In one embodiment, the reaction entity is attached to the nanoscale wire through a linker.

As used herein, "attached to," in the context of a species relative to another species or to a surface of an article, means that the species is chemically or biochemically linked via covalent attachment, attachment via specific biological binding (e.g., biotin/streptavidin), coordinative bonding such as chelate/metal binding, or the like. For example, "attached" in this context includes multiple chemical linkages, multiple

chemical/biological linkages, etc., for example, a binding species such as a peptide synthesized on a polystyrene bead. "Covalently attached" means attached via one or more covalent bonds.

Another set of embodiments of the invention involve an article comprising a sample exposure region and one or more nanoscale wires able to detect the presence of absence of an analyte. In some cases, a plurality of aligned nanoscale wires may be present. The sample exposure region may be any region in close proximity to the nanoscale wires wherein a sample in the sample exposure region addresses at least a portion of the nanoscale wires. Examples of sample exposure regions include, but are not limited to, a well, a channel, a microchannel, and a gel. In some embodiments, the sample exposure region holds a sample proximate the nanoscale wires, or may direct a sample toward the nanoscale wire for determination of an analyte in the sample. The nanoscale wires may be positioned adjacent to or within the sample exposure region. Alternatively, the nanoscale wires may define a probe that is inserted into a fluid or fluid flow path. The nanoscale wires may also comprise a micro-needle and the sample exposure region may be addressable by a biological sample. In this arrangement, a device that is constructed and arranged for insertion of a micro-needle probe into a biological sample will include a region surrounding the micro-needle that defines the sample exposure region, and a sample in the sample exposure region is addressable by the nanoscale wires, and/or vice versa. Fluid flow channels can be created at a size and scale advantageous for use in the invention (microchannels) using a variety of techniques such as those described in International Patent Publication No. WO 97/33737, published September 18, 1997, and incorporated herein by reference.

Where a detector is present, any detector capable of determining a property associated with a nanoscale wire can be used, which can be used to determine the analyte. The property can be electronic, optical, or the like. An electronic property of a nanoscale wire can be, for example, its conductivity, resistivity, etc. An optical property associated with a nanoscale wire can include its emission intensity, or emission wavelength where the nanoscale wire is an emissive nanoscale wire where emission occurs at a p-n junction. For example, the detector can be constructed for measuring a change in an electronic or magnetic property (e.g. voltage, current, conductivity, resistance, impedance, inductance, charge, etc.) can be used. The detector typically

includes a power source and a voltmeter or amp meter. In one embodiment, a conductance less than 1 nS can be detected. In a preferred embodiment, a conductance in the range of thousandths of a nS can be detected. The concentration of a species, or analyte, may be detected from less than micromolar to molar concentrations and above. By using nanoscale wires with known detectors, sensitivity can be extended to a single molecule. In one embodiment, an article of the invention is capable of delivering a stimulus to a nanoscale wire and the detector is constructed and arranged to determine a signal resulting from the stimulus. For example, a nanoscale wire including a p-n junction can be delivered a stimulus (electronic current), where the detector is constructed and arranged to determine a signal (electromagnetic radiation) resulting from the stimulus. In such an arrangement, interaction of an analyte with the nanoscale wire, or with a reaction entity positioned proximate the nanoscale wire, can affect the signal in a detectable manner. In another example, where the reaction entity is a quantum dot, the quantum dot may be constructed to receive electromagnetic radiation of one wavelength and emit electromagnetic radiation of a different wavelength. Where the stimulus is electromagnetic radiation, it can be affected by interaction with an analyte, and the detector can detect a change in a signal resulting therefrom. Examples of stimuli include a constant current/voltage, an alternating voltage, and electromagnetic radiation such as light.

A nanoscale sensor of the present invention can collect real time data. The real time data may be used, for example; to monitor the reaction rate of a specific chemical or biological reaction. Physiological conditions or drug concentrations present in vivo may also produce a real time signal that may be used to control a drug delivery system. For example, the present invention includes, in one set of embodiments, an integrated system, comprising a nanoscale wire detector, a reader and a computer controlled response system. In this example, the nanoscale wire detects a change in the equilibrium of an analyte in the sample, feeding a signal to the computer controlled response system causing it to withhold or release a chemical or drug. This is particularly useful as an implantable drug or chemical delivery system because of its small size and low energy requirements. Those of ordinary skill in the art are well aware of the parameters and requirements for constructing implantable devices, readers, and computer-controlled response systems suitable for use in connection with the present invention. That is, the

knowledge of those of ordinary skill in the art, coupled with the disclosure herein of nanoscale wires as sensors, enables implantable devices, real-time measurement devices, integrated systems, and the like. Such systems can be made capable of monitoring one, or a plurality of physiological characteristics individually or simultaneously. Such physiological characteristics can include, for example, oxygen concentration, carbon dioxide concentration, glucose level, concentration of a particular drug, concentration of a particular drug by-product, or the like. Integrated physiological devices can be constructed to carry out a function depending upon a condition sensed by a sensor of the invention. For example, a nanoscale wire sensor of the invention can sense glucose level and, based upon the determined glucose level can cause the release of insulin into a subject through an appropriate controller mechanism.

In another embodiment, the article may comprise a cassette comprising a sample exposure region and one or more nanoscale wires, which may be aligned in some instances. The detection of an analyte in a sample in the sample exposure region may occur while the cassette is disconnected to a detector apparatus, allowing samples to be gathered at one site, and detected at another. The cassette may be operatively connectable to a detector apparatus able to determine a property associated with the nanoscale wire. As used herein, a device is "operatively connectable" when it has the ability to attach and interact with another apparatus.

In another embodiment, one or more nanoscale wires may be positioned in a microfluidic channel, and in some cases, the nanoscale wires may be aligned. One or more nanoscale wires may cross the same microchannel at different positions to detect a different analyte or to measure flow rate of the same analyte. In another embodiment, one or more nanoscale wires positioned in a microfluidic channel may form one of a plurality of analytic elements in a microneedle probe or a dip and read probe. The microneedle probe is implantable and capable of detecting several analytes simultaneously in real time. In another embodiment, one or more nanoscale wires positioned in a microfluidic channel may form one of the analytic elements in a microarray for a cassette or a lab on a chip device. Those skilled in the art would know such cassette or lab on a chip device will be in particular suitable for high throughout chemical analysis and combinational drug discovery. Moreover, the associated method of using the nanoscale sensor is fast and simple, in that it does not require labeling as in

other sensing techniques. The ability to include multiple nanoscale wires in one nanoscale sensor, also allows for the simultaneous detection of different analytes suspected of being present in a single sample. For example, a nanoscale pH sensor may include a plurality of nanoscale wires that each detect different pH levels, or a nanoscale oligonucleotide sensor with multiple nanoscale wires may be used to detect multiple sequences, or combination of sequences.

In one aspect, the present invention provides any of the above-mentioned devices packaged in kits, optionally including instructions for use of the devices. As used herein, "instructions" can define a component of instructional utility (e.g., directions, guides, warnings, labels, notes, FAQs ("frequently asked questions"), etc., and typically involve written instructions on or associated with packaging of the invention. Instructions can also include instructional communications in any form (e.g., oral, electronic, digital, optical, visual, etc.), provided in any manner such that a user will clearly recognize that the instructions are to be associated with the device, e.g., as discussed herein. Additionally, the kit may include other components depending on the specific application, for example, containers, adapters, syringes, needles, replacement parts, etc. As used herein, "promoted" includes all methods of doing business including, but not limited to, methods of selling, advertising, assigning, licensing, contracting, instructing, educating, researching, importing, exporting, negotiating, financing, loaning, trading, vending, reselling, distributing, replacing, or the like that can be associated with the methods and compositions of the invention, e.g., as discussed herein. Promoting may also include, in some cases, seeking approval from a government agency to sell a composition of the invention for medicinal purposes. Methods of promotion can be performed by any party including, but not limited to, businesses (public or private), contractual or sub-contractual agencies, educational institutions such as colleges and universities, research institutions, hospitals or other clinical institutions, governmental agencies, etc. Promotional activities may include instructions or communications of any form (e.g., written, oral, and/or electronic communications, such as, but not limited to, e-mail, telephonic, facsimile, Internet, Web-based, etc.) that are clearly associated with the invention.

Definitions

The following definitions will aid in the understanding of the invention. Interspersed with these definitions is additional disclosure of various embodiments of the invention.

Certain devices of the invention may include wires or other components of scale commensurate with nanometer-scale wires, which includes nanotubes and nanowires. In some embodiments, however, the invention comprises articles that may be greater than nanometer size (e. g., micrometer-sized). As used herein, "nanoscopic-scale," "nanoscopic," "nanometer-scale," "nanoscale," the "nano-" prefix (for example, as in "nanostructured"), and the like generally refers to elements or articles having widths or diameters of less than about 1 micron, and less than about 100 nm in some cases. In all embodiments, specified widths can be a smallest width (i.e. a width as specified where, at that location, the article can have a larger width in a different dimension), or a largest width (i.e. where, at that location, the article has a width that is no wider than as specified, but can have a length that is greater).

As used herein, a "wire" generally refers to any material having a conductivity of or of similar magnitude to any semiconductor or any metal, and in some embodiments may be used to connect two electronic components such that they are in electronic communication with each other. For example, the terms "electrically conductive" or a "conductor" or an "electrical conductor" when used with reference to a "conducting" wire or a nanoscale wire, refers to the ability of that wire to pass charge. Typically, an electrically conductive nanoscale wire will have a resistivity comparable to that of metal or semiconductor materials, and in some cases, the electrically conductive nanoscale wire may have lower resistivities, for example, resistivities of less than about 100 microOhm cm ($\mu\Omega$ cm). In some cases, the electrically conductive nanoscale wire will have a resistivity lower than about 10^{-3} ohm meters, lower than about 10^{-4} ohm meters, or lower than about 10^{-6} ohm meters or 10^{-7} ohm meters.

A "semiconductor," as used herein, is given its ordinary meaning in the art, i.e., an element having semiconductive or semi-metallic properties (i.e., between metallic and non-metallic properties). An example of a semiconductor is silicon. Other non-limiting examples include gallium, germanium, diamond (carbon), tin, selenium, tellurium, boron, or phosphorous.

A "nanoscopic wire" (also known herein as a "nanoscopic-scale wire" or "nanoscale wire") generally is a wire, that at any point along its length, has at least one cross-sectional dimension and, in some embodiments, two orthogonal cross-sectional dimensions less than 1 micron, less than about 500 nm, less than about 200 nm, less than about 150 nm, less than about 100 nm, less than about 70, less than about 50 nm, less than about 20 nm, less than about 10 nm, or less than about 5 nm. In other embodiments, the cross-sectional dimension can be less than 2 nm or 1 nm. In one set of embodiments, the nanoscale wire has at least one cross-sectional dimension ranging from 0.5 nm to 100 nm or 200 nm. In some cases, the nanoscale wire is electrically conductive. Where nanoscale wires are described having, for example, a core and an outer region, the above dimensions generally relate to those of the core. The cross-section of a nanoscopic wire may be of any arbitrary shape, including, but not limited to, circular, square, rectangular, annular, polygonal, or elliptical, and may be a regular or an irregular shape. The nanoscale wire may be solid or hollow. A non-limiting list of examples of materials from which nanoscale wires of the invention can be made appears below. Any nanoscale wire can be used in any of the embodiments described herein, including carbon nanotubes, molecular wires (i.e., wires formed of a single molecule), nanorods, nanowires, nanowhiskers, organic or inorganic conductive or semiconducting polymers, and the like, unless otherwise specified. Other conductive or semiconducting elements that may not be molecular wires, but are of various small nanoscopic-scale dimensions, can also be used in some instances, e.g. inorganic structures such as main group and metal atom-based wire-like silicon, transition metal-containing wires, gallium arsenide, gallium nitride, indium phosphide, germanium, cadmium selenide, etc. A wide variety of these and other nanoscale wires can be grown on and/or applied to surfaces in patterns useful for electronic devices in a manner similar to techniques described herein involving the specific nanoscale wires used as examples, without undue experimentation. The nanoscale wires, in some cases, may be formed having dimensions of at least about 1 micron, at least about 3 microns, at least about 5 microns, or at least about 10 microns or about 20 microns in length, and can be less than about 100 nm, less than about 80 nm, less than about 60 nm, less than about 40 nm, less than about 20 nm, less than about 10 nm, or less than about 5 nm in thickness (height and width). The nanoscale wires may have an aspect ratio (length to thickness) of greater than about 2:1, greater than about

3:1, greater than about 4:1, greater than about 5:1, greater than about 10:1, greater than about 25:1, greater than about 50:1, greater than about 75:1, greater than about 100:1, greater than about 150:1, greater than about 250:1, greater than about 500:1, greater than about 750:1, or greater than about 1000:1 or more in some cases.

A "nanowire" (e. g. comprising silicon and/or another semiconductor material) is a nanoscopic wire that is typically a solid wire, and may be elongated in some cases. Preferably, a nanowir (which is abbreviated herein as "NW") is an elongated semiconductor, i.e., a nanoscale semiconductor. A "non-nanotube nanowire" is any nanowire that is not a nanotube. In one set of embodiments of the invention, a non-nanotube nanowire having an unmodified surface (not including an auxiliary reaction entity not inherent in the nanotube in the environment in which it is positioned) is used in any arrangement of the invention described herein in which a nanowire or nanotube can be used.

As used herein, a "nanotube" (e.g. a carbon nanotube) is a nanoscopic wire that is hollow, or that has a hollowed-out core, including those nanotubes known to those of ordinary skill in the art. "Nanotube" is abbreviated herein as "NT." Nanotubes are used as one example of small wires for use in the invention and, in certain embodiments, devices of the invention include wires of scale commensurate with nanotubes. Examples of nanotubes that may be used in the present invention include, but are not limited to, single-walled nanotubes (SWNTs). Structurally, SWNTs are formed of a single graphene sheet rolled into a seamless tube. Depending on the diameter and helicity, SWNTs can behave as one-dimensional metals and/or semiconductors. SWNTs. Methods of manufacture of nanotubes, including SWNTs, and characterization are known. Methods of selective functionalization on the ends and/or sides of nanotubes also are known, and the present invention makes use of these capabilities for molecular electronics in certain embodiments. Multi-walled nanotubes are well known, and can be used as well.

Examples of nanotubes that may be used in the present invention include single-walled nanotubes (SWNTs) that exhibit unique electronic, and chemical properties that are particularly suitable for molecular electronics. Structurally, SWNTs are formed of a single graphene sheet rolled into a seamless tube with a diameter on the order of about 0.5 nm to about 5 nm and a length that can exceed about 10 microns. Depending on

diameter and helicity, SWNTs can behave as one-dimensional metals or semiconductor and are currently available as a mixture of metallic and semiconducting nanotubes. Methods of manufacture of nanotubes, including SWNTs, and characterization are known. Methods of selective functionalization on the ends and/or sides of nanotubes also are known, and the present invention makes use of these capabilities for molecular electronics. The basic structural/electronic properties of nanotubes can be used to create connections or input/output signals, and nanotubes have a size consistent with molecular scale architecture.

Certain nanoscale wires of the present invention are individual nanoscale wires. As used herein, "individual nanoscale wires" means a nanoscale wire free of contact with another nanoscale wire (but not excluding contact of a type that may be desired between individual nanoscale wires in a crossbar array). For example, typical individual nanoscale wire can have a thickness as small as about 0.5 nm. This is in contrast to nanoscale wires produced primarily by laser vaporization techniques that produce high-quality materials, but materials formed as ropes having diameters of about 2 to about 50 nanometers or more and containing many individual nanoscale wires (see, for example, Thess, *et al.*, "Crystalline Ropes of Metallic Carbon Nanotubes" *Science* 273, 483-486 (1996), incorporated herein by reference). While nanoscale wire ropes can be used in the invention, individual nanoscale wires are preferred.

The invention may utilize metal-catalyzed CVD to synthesize high quality individual nanoscale wires such as nanotubes for molecular electronics. CVD synthetic procedures needed to prepare individual wires directly on surfaces and in bulk form are known, and can readily be carried out by those of ordinary skill in the art. See, for example, Kong, *et al.*, "Synthesis of Individual Single-Walled Carbon Nanotubes on Patterned Silicon Wafers", *Nature* 395, 878-881 (1998); Kong, *et al.*, "Chemical Vapor Deposition of Methane for Single-Walled Carbon Nanotubes" *Chem. Phys. Lett.* 292, 567-574 (1998), both incorporated herein by reference. Nanoscale wires may also be grown through laser catalytic growth. See, for example, Morales *et al.* "A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanoscale wires" *Science* 279, 208-211 (1998), incorporated herein by reference.

In other embodiments, the nanoscale wire may comprise a semiconductor that is doped with an appropriate dopant to create an n-type or p-type semiconductor as desired.

For example, silicon may be doped with boron, aluminum, phosphorous, or arsenic. Laser catalytic growth may be used to introduce controllably the dopants during the vapor phase growth of silicon nanoscale wires.

Controlled doping of nanoscale wires can be carried out to form, e.g., n-type or p-type semiconductors. In various embodiments, this invention involves controlled doping of semiconductors selected from among indium phosphide, gallium arsenide, gallium nitride, cadmium selenide, and zinc selenide. Dopants including, but not limited to, zinc, cadmium, or magnesium can be used to form p-type semiconductors in this set of embodiments, and dopants including, but not limited to, tellurium, sulfur, selenium, or germanium can be used as dopants to form n-type semiconductors from these materials. These materials define direct band gap semiconductor materials and these and doped silicon are well known to those of ordinary skill in the art. The present invention contemplates use of any doped silicon or direct band gap semiconductor materials for a variety of uses, as discussed above.

Some embodiments of the invention include nanoscopic wires, each of which can be any nanoscopic wire, including nanorods, nanowires, organic and inorganic conductive and semiconducting polymers, nanotubes, semiconductor components or pathways and the like. Other nanoscopic-scale conductive or semiconducting elements that may be used in some instances include, for example, inorganic structures such as Group IV, Group III/Group V, Group II/Group VI elements, transition group elements, or the like, as described below. For example, the nanoscale wires may be made of semiconducting materials such as silicon, indium phosphide, gallium nitride and others. The nanoscale wires may also include, for example, any organic, inorganic molecules that are polarizable or have multiple charge states. For example, nanoscopic-scale structures may include main group and metal atom-based wire-like silicon, transition metal-containing wires, gallium arsenide, gallium nitride, indium phosphide, germanium, or cadmium selenide structures.

The nanoscale wires may include various combinations of materials, including semiconductors and dopants. The following are non-comprehensive examples of materials that may be used as dopants. For example, the dopant may be an elemental semiconductor, for example, silicon, germanium, tin, selenium, tellurium, boron, diamond, or phosphorous. The dopant may also be a solid solution of various elemental

semiconductors. Examples include a mixture of boron and carbon, a mixture of boron and $P(BP_6)$, a mixture of boron and silicon, a mixture of silicon and carbon, a mixture of silicon and germanium, a mixture of silicon and tin, or a mixture of germanium and tin.

In some embodiments, the dopant or the semiconductor may include mixtures of Group IV elements, for example, a mixture of silicon and carbon, or a mixture of silicon and germanium. In other embodiments, the dopant or the semiconductor may include a mixture of a Group III and a Group V element, for example, BN, BP, BAs, AlN, AlP, AlAs, AlSb, GaN, GaP, GaAs, GaSb, InN, InP, InAs, or InSb. Mixtures of these may also be used, for example, a mixture of BN/BP/BAs, or BN/AlP. In other embodiments, the dopants may include alloys of Group III and Group V elements. For example, the alloys may include a mixture of AlGaN, GaPAs, InPAs, GaInN, AlGaInN, GaInAsP, or the like. In other embodiments, the dopants may also include a mixture of Group II and Group VI semiconductors. For example, the semiconductor may include ZnO, ZnS, ZnSe, ZnTe, CdS, CdSe, CdTe, HgS, HgSe, HgTe, BeS, BeSe, BeTe, MgS, MgSe, or the like. Alloys or mixtures of these dopants are also be possible, for example, (ZnCd)Se, or Zn(SSe), or the like. Additionally, alloys of different groups of semiconductors may also be possible, for example, a combination of a Group II-Group VI and a Group III-Group V semiconductor, for example, $(GaAs)_x(ZnS)_{1-x}$. Other examples of dopants may include combinations of Group IV and Group VI elemnts, such as GeS, GeSe, GeTe, SnS, SnSe, SnTe, PbO, PbS, PbSe, or PbTe. Other semiconductor mixtures may include a combination of a Group I and a Group VII, such as CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI, or the like. Other dopant compounds may include different mixtures of these elements, such as $BeSiN_2$, $CaCN_2$, $ZnGeP_2$, $CdSnAs_2$, $ZnSnSb_2$, $CuGeP_3$, $CuSi_2P_3$, Si_3N_4, Ge_3N_4, Al_2O_3, $(Al,Ga,In)_2(S,Se,Te)_3$, Al_2CO, $(Cu,Ag)(Al,Ga,In,Tl,Fe)(S,Se,Te)_2$ and the like.

For Group IV dopant materials, a p-type dopant may be selected from Group III, and an n-type dopant may be selected from Group V, for example. For silicon semiconductor materials, a p-type dopant may be selected from the group consisting of B, Al and In, and an n-type dopant may be selected from the group consisting of P, As and Sb. For Group III-Group V semiconductor materials, a p-type dopant may be selected from Group II, including Mg, Zn, Cd and Hg, or Group IV, including C and Si. An n-type dopant may be selected from the group consisting of Si, Ge, Sn, S, Se and Te.

It will be understood that the invention is not limited to these dopants, but may include other elements, alloys, or materials as well.

Controlled doping of nanoscale wires can be carried out to form, e.g., n-type or p-type semiconductors. One set of embodiments involves use of at least one semiconductor, controllably-doped with a dopant (e.g., boron, aluminum, phosphorous, arsenic, etc.) selected according to whether an n-type or p-type semiconductor is desired. A bulk-doped semiconductor may include various combinations of materials, including other semiconductors and dopants. For instance, the nanoscopic wire may be a semiconductor that is doped with an appropriate dopant to create an n-type or p-type semiconductor, as desired. As one example, silicon may be doped with boron, aluminum, phosphorous, or arsenic. In various embodiments, this invention involves controlled doping of semiconductors selected from among indium phosphide, gallium arsenide, gallium nitride, cadmium selenide. Dopants including, but not limited to, zinc, cadmium, or magnesium can be used to form p-type semiconductors in this set of embodiments, and dopants including, but not limited to, tellurium, sulfur, selenium, or germanium can be used as dopants to form n-type semiconductors from these materials. These materials may define direct band gap semiconductor materials and these and doped silicon are well known to those of ordinary skill in the art.. The present invention contemplates use of any doped silicon or direct band gap semiconductor materials for a variety of uses.

As used herein, an "elongated" article (e.g. a semiconductor or a section thereof) is an article for which, at any point along the longitudinal axis of the article, the ratio of the length of the article to the largest width at that point is greater than 2:1.

A "width" of an article, as used herein, is the distance of a straight line from a point on a perimeter of the article, through the center of the article, to another point on the perimeter of the article. As used herein, a "width" or a "cross-sectional dimension" at a point along a longitudinal axis of an article is the distance along a straight line that passes through the center of a cross-section of the article at that point and connects two points on the perimeter of the cross-section. The "cross-section" at a point along the longitudinal axis of an article is a plane at that point that crosses the article and is orthogonal to the longitudinal axis of the article. The "longitudinal axis" of an article is the axis along the largest dimension of the article. Similarly, a "longitudinal section" of

an article is a portion of the article along the longitudinal axis of the article that can have any length greater than zero and less than or equal to the length of the article. Additionally, the "length" of an elongated article is a distance along the longitudinal axis from end to end of the article.

As used herein, a "cylindrical" article is an article having an exterior shaped like a cylinder, but does not define or reflect any properties regarding the interior of the article. In other words, a cylindrical article may have a solid interior, may have a hollowed-out interior, etc. Generally, a cross-section of a cylindrical article appears to be circular or approximately circular, but other cross-sectional shapes are also possible, such as a hexagonal shape. The cross-section may have any arbitrary shape, including, but not limited to, square, rectangular, or elliptical. Regular and irregular shapes are also included.

As used herein, an "array" of articles (e.g., nanoscopic wires) comprises a plurality of the articles, for example, a series of aligned nanoscale wires, which may or may not be in contact with each other. As used herein, a "crossed array" or a "crossbar array" is an array where at least one of the articles contacts either another of the articles or a signal node (e.g., an electrode).

"Determine," as used herein, generally refers to the analysis of a state or condition, for example, quantitatively or qualitatively. For example, a species, or an electrical state of a system may be determined. "Determining" may also refer to the analysis of an interaction between two or more species, for example, quantitatively or qualitatively, and/or by detecting the presence or absence of the interaction, e.g. determination of the binding between two species. As an example, an analyte may cause a determinable change in an electrical property of a nanoscale wire (e.g., electrical conductivity, resistivity, impedance, etc.), a change in an optical property of the nanoscale wire, etc. Examples of determination techniques include, but are not limited to, conductance measurement, current measurement, voltage measurement, resistance measurement, piezoelectric measurement, electrochemical measurement, electromagnetic measurement, photodetection, mechanical measurement, acoustic measurement, gravimetric measurement, and the like. "Determining" also means detecting or quantifying interaction between species.

A "fluid," as used herein, generally refers to a substance that tends to flow and to conform to the outline of its container. Typically, fluids are materials that are unable to withstand a static shear stress. When a shear stress is applied to a fluid, it experiences a continuing and permanent distortion. Typical fluids include liquids and gases, but may also include free-flowing solid particles, viscoelastic fluids, and the like.

As used herein, a component that is "immobilized relative to" another component either is fastened to the other component or is indirectly fastened to the other component, e.g., by being fastened to a third component to which the other component also is fastened. For example, a first entity is immobilized relative to a second entity if a species fastened to the surface of the first entity attaches to an entity, and a species on the surface of the second entity attaches to the same entity, where the entity can be a single entity, a complex entity of multiple species, another particle, etc. In certain embodiments, a component that is immobilized relative to another component is immobilized using bonds that are stable, for example, in solution or suspension. In some embodiments, non-specific binding of a component to another component, where the components may easily separate due to solvent or thermal effects, is not preferred.

As used herein, "fastened to or adapted to be fastened to," as used in the context of a species relative to another species or a species relative to a surface of an article (such as a nanoscale wire), or to a surface of an article relative to another surface, means that the species and/or surfaces are chemically or biochemically linked to or adapted to be linked to, respectively, each other via covalent attachment, attachment via specific biological binding (e.g., biotin/streptavidin), coordinative bonding such as chelate/metal binding, or the like. For example, "fastened" in this context includes multiple chemical linkages, multiple chemical/biological linkages; etc., including, but not limited to, a binding species such as a peptide synthesized on a nanoscale wire, a binding species specifically biologically coupled to an antibody which is bound to a protein such as protein A, which is attached to a nanoscale wire, a binding species that forms a part of a molecule, which in turn is specifically biologically bound to a binding partner covalently fastened to a surface of a nanoscale wire, etc. A species also is adapted to be fastened to a surface if a surface carries a particular nucleotide sequence, and the species includes a complementary nucleotide sequence.

"Specifically fastened" or "adapted to be specifically fastened" means a species is chemically or biochemically linked to or adapted to be linked to, respectively, another specimen or to a surface as described above with respect to the definition of "fastened to or adapted to be fastened," but excluding essentially all non-specific binding. "Covalently fastened" means fastened via essentially nothing other than one or more covalent bonds.

The term "binding" refers to the interaction between a corresponding pair of molecules or surfaces that exhibit mutual affinity or binding capacity, typically due to specific or non-specific binding or interaction, including, but not limited to, biochemical, physiological, and/or chemical interactions. "Biological binding" defines a type of interaction that occurs between pairs of molecules including proteins, nucleic acids, glycoproteins, carbohydrates, hormones and the like. Specific non-limiting examples include antibody/antigen, antibody/hapten, enzyme/substrate, enzyme/inhibitor, enzyme/cofactor, binding protein/substrate, carrier protein/substrate, lectin/carbohydrate, receptor/hormone, receptor/effector, complementary strands of nucleic acid, protein/nucleic acid repressor/inducer, ligand/cell surface receptor, virus/ligand, virus/cell surface receptor, etc.

The term "binding partner" refers to a molecule that can undergo binding with a particular molecule. Biological binding partners are examples. For example, Protein A is a binding partner of the biological molecule IgG, and vice versa. Other non-limiting examples include nucleic acid-nucleic acid binding, nucleic acid-protein binding, protein-protein binding, enzyme-substrate binding, receptor-ligand binding, receptor-hormone binding, antibody-antigen binding, etc. Binding partners include specific, semi-specific, and non-specific binding partners as known to those of ordinary skill in the art. For example, Protein A is usually regarded as a "non-specific" or semi-specific binder. The term "specifically binds," when referring to a binding partner (e.g., protein, nucleic acid, antibody, etc.), refers to a reaction that is determinative of the presence and/or identity of one or other member of the binding pair in a mixture of heterogeneous molecules (e.g., proteins and other biologics). Thus, for example, in the case of a receptor/ligand binding pair the ligand would specifically and/or preferentially select its receptor from a complex mixture of molecules, or vice versa. An enzyme would specifically bind to its substrate, a nucleic acid would specifically bind to its

complement, an antibody would specifically bind to its antigen. Other examples include nucleic acids that specifically bind (hybridize) to their complement, antibodies specifically bind to their antigen, binding pairs such as those described above, and the like. The binding may be by one or more of a variety of mechanisms including, but not limited to ionic interactions, and/or covalent interactions, and/or hydrophobic interactions, and/or van der Waals interactions, etc.

The terms "polypeptide," "peptide," and "protein" are used interchangeably herein to refer to a polymer of amino acid residues. The terms apply to amino acid polymers in which one or more amino acid residue is an artificial chemical analogue of a corresponding naturally occurring amino acid, as well as to naturally occurring amino acid polymers. The term also includes variants on the traditional peptide linkage joining the amino acids making up the polypeptide.

As used herein, terms such as "polynucleotide" or "oligonucleotide" or grammatical equivalents generally refer to a polymer of at least two nucleotide bases covalently linked together, which may include, for example, but not limited to, natural nucleosides (e.g., adenosine, thymidine, guanosine, cytidine, uridine, deoxyadenosine, deoxythymidine, deoxyguanosine and deoxycytidine), nucleoside analogs (e.g., 2-aminoadenosine, 2-thiothymidine, inosine, pyrrolopyrimidine, 3-methyladenosine, C5-bromouridine, C5-fluorouridine, C5-iodouridine, C5-propynyluridine, C5-propynylcytidine, C5-methylcytidine, 7-deazaadenosine, 7-deazaguanosine, 8-oxoadenosine, 8-oxoguanosine, O6-methylguanosine, 2-thiocytidine, 2-aminopurine, 2-amino-6-chloropurine, 2,6-diaminopurine, hypoxanthine), chemically or biologically modified bases (e.g., methylated bases), intercalated bases, modified sugars (2'-fluororibose, arabinose, or hexose), modified phosphate moieties (e.g., phosphorothioates or 5'-N-phosphoramidite linkages), and/or other naturally and non-naturally occurring bases substitutable into the polymer, including substituted and unsubstituted aromatic moieties. Other suitable base and/or polymer modifications are well-known to those of skill in the art. Typically, an "oligonucleotide" is a polymer having 20 bases or less, and a "polynucleotide" is a polymer having at least 20 bases. Those of ordinary skill in the art will recognize that these terms are not precisely defined in terms of the number of bases present within the polymer strand.

A "nucleic acid," as used herein, is given its ordinary meaning as used in the art. Nucleic acids can be single-stranded or double stranded, and will generally contain phosphodiester bonds, although in some cases, as outlined below, nucleic acid analogs are included that may have alternate backbones, comprising, for example, phosphoramide (Beaucage *et al.* (1993) *Tetrahedron* 49(10):1925) and references therein; Letsinger (1970) *J. Org. Chem.* 35:3800; Sprinzl *et al.* (1977) *Eur. J. Biochem.* 81: 579; Letsinger *et al.* (1986) *Nucl. Acids Res.* 14: 3487; Sawai *et al.* (1984) *Chem. Lett.* 805, Letsinger *et al.* (1988) *J. Am. Chem. Soc.* 110: 4470; and Pauwels *et al.* (1986) *Chemica Scripta* 26: 1419, phosphorothioate (Mag *et al.* (1991) *Nucleic Acids Res.* 19:1437; and U.S. Patent No. 5,644,048), phosphorodithioate (Briu *et al.* (1989) *J. Am. Chem. Soc.* 111:2321), O-methylphophoroamidite linkages (*see* Eckstein, *Oligonucleotides and Analogues: A Practical Approach*, Oxford University Press), and peptide nucleic acid backbones and linkages (*see* Egholm (1992) *J. Am. Chem. Soc.* 114:1895; Meier *et al.* (1992) *Chem. Int. Ed. Engl.* 31: 1008; Nielsen (1993) *Nature*, 365: 566; Carlsson *et al.* (1996) *Nature* 380: 207). Other analog nucleic acids include those with positive backbones (Denpcy *et al.* (1995) *Proc. Natl. Acad. Sci. USA* 92: 6097); non-ionic backbones (U.S. Patent Nos. 5,386,023, 5,637,684, 5,602,240, 5,216,141 and 4,469,863; Angew. (1991) *Chem. Intl. Ed. English* 30: 423; Letsinger *et al.* (1988) *J. Am. Chem. Soc.* 110:4470; Letsinger *et al.* (1994) *Nucleoside & Nucleotide* 13:1597; Chapters 2 and 3, ASC Symposium Series 580, "Carbohydrate Modifications in Antisense Research", Ed. Y.S. Sanghui and P. Dan Cook; Mesmaeker *et al.* (1994), *Bioorganic & Medicinal Chem. Lett.* 4: 395; Jeffs *et al.* (1994) *J. Biomolecular NMR* 34:17; *Tetrahedron Lett.* 37:743 (1996)) and non-ribose backbones, including those described in U.S. Patent Nos. 5,235,033 and 5,034,506, and Chapters 6 and 7, ASC Symposium Series 580, *Carbohydrate Modifications in Antisense Research*, Ed. Y.S. Sanghui and P. Dan Cook. Nucleic acids containing one or more carbocyclic sugars are also included within the definition of nucleic acids (see Jenkins *et al.* (1995), *Chem. Soc. Rev.* pp. 169-176). Several nucleic acid analogs are described in Rawls, *Chemical & Engineering News*, June 2, 1997 page 35. These modifications of the ribose-phosphate backbone may be done to facilitate the addition of additional moieties such as labels, or to increase the stability and half-life of such molecules in physiological environments.

As used herein, an "antibody" refers to a protein or glycoprotein including one or more polypeptides substantially encoded by immunoglobulin genes or fragments of immunoglobulin genes. The recognized immunoglobulin genes include the kappa, lambda, alpha, gamma, delta, epsilon and mu constant region genes, as well as myriad immunoglobulin variable region genes. Light chains are classified as either kappa or lambda. Heavy chains are classified as gamma, mu, alpha, delta, or epsilon, which in turn define the immunoglobulin classes, IgG, IgM, IgA, IgD and IgE, respectively. A typical immunoglobulin (antibody) structural unit is known to comprise a tetramer. Each tetramer is composed of two identical pairs of polypeptide chains, each pair having one "light" (about 25 kD) and one "heavy" chain (about 50-70 kD). The N-terminus of each chain defines a variable region of about 100 to 110 or more amino acids primarily responsible for antigen recognition. The terms variable light chain (VL) and variable heavy chain (VH) refer to these light and heavy chains respectively. Antibodies exist as intact immunoglobulins or as a number of well characterized fragments produced by digestion with various peptidases. Thus, for example, pepsin digests an antibody below (*i.e.* toward the Fc domain) the disulfide linkages in the hinge region to produce F(ab)'2, a dimer of Fab which itself is a light chain joined to V_H-C_H1 by a disulfide bond. The F(ab)'2 may be reduced under mild conditions to break the disulfide linkage in the hinge region thereby converting the (Fab')2 dimer into an Fab' monomer. The Fab' monomer is essentially a Fab with part of the hinge region (see, Paul (1993) *Fundamental Immunology,* Raven Press, N.Y. for a more detailed description of other antibody fragments). While various antibody fragments are defined in terms of the digestion of an intact antibody, one of skill will appreciate that such fragments may be synthesized de novo either chemically, by utilizing recombinant DNA methodology, or by "phage display" methods (see, e.g., Vaughan *et al.* (1996) *Nature Biotechnology,* 14(3): 309-314, and PCT/US96/10287). Preferred antibodies include single chain antibodies, e.g., single chain Fv (scFv) antibodies in which a variable heavy and a variable light chain are joined together (directly or through a peptide linker) to form a continuous polypeptide.

The term "quantum dot" is known to those of ordinary skill in the art, and generally refers to semiconductor or metal nanoparticles that absorb light and quickly re-emit light in a different color depending on the size of the dot. For example, a 2 nanometer quantum dot emits green light, while a 5 nanometer quantum dot emits red

light. Cadmium selenide quantum dot nanocrystals are available from Quantum Dot Corporation of Hayward, California.

The following documents are each incorporated herein by reference: U.S. Patent Application Serial No. 09/935,776, filed August 22, 2001, entitled "Doped Elongated Semiconductors, Growing Such Semiconductors, Devices Including Such Semiconductors, and Fabricating Such Devices," by Lieber, *et al.*, published as U.S. Patent Application Publication No. 2002/0130311 on September 19, 2002; U.S. Patent Application Serial No. 10/020,004, filed December 11, 2001, entitled "Nanosensors," by Lieber, *et al.*, published as U.S. Patent Application Publication No. 2002/0117659 on August 29, 2002; U.S. Patent Application Serial No. 10/196,337, filed July 16, 2002, entitled "Nanoscale Wires and Related Devices," by Lieber, *et al.*, published as U.S. Patent Application Publication No. 2003/0089899 on May 15, 2003; U.S. Patent Application Serial No. 10/995,075, filed November 22, 2004, entitled "Nanoscale Arrays, Robust Nanostructures, and Related Devices," by Whang, *et al.*, published as U.S. Patent Application Publication No. 2005/0253137 on November 17, 2005; U.S. Provisional Patent Application Serial No. 60/551,634, filed March 8, 2004, entitled "Robust Nanostructures," by McAlpine, *et al.*; International Patent Application No. PCT/US2005/004459, filed February 14, 2005, entitled "Nanostructures Containing Metal-Semiconductor Compounds," by Lieber, *et al.*, published as WO 2005/093831 on October 6, 2005; International Patent Application No. PCT/US2005/020974, filed June 15, 2005, entitled "Nanosensors," by Wang, *et al.*; U.S. Patent Application Serial No. 11/137,784, filed May 25, 2005, entitled "Nanoscale Sensors," by Lieber, *et al.*; an International Patent Application filed September 21, 2005, entitled "Nanowire Heterostructures," by Lu, *et al.*; U.S. Provisional Patent Application Serial No. 60/707,136, filed August 9, 2005, entitled "Nanoscale Sensors," by Lieber, *et al.*; and U.S. Provisional Patent Application Serial No. 60/790,322, filed April 7, 2006, entitled "Nanoscale Wire Methods and Devices," by Lieber, *et al.*

The following examples are intended to illustrate certain embodiments of the present invention, but do not exemplify the full scope of the invention.

EXAMPLE 1

In this example, an array of devices were prepared using the systems and methods of one embodiment of the invention. Referring now to Fig. 2, on a first, growth

substrate 10, a series of germanium and silicon nanowires 15 were grown substantially perpendicular to the surface of the substrate orientation using techniques known to those of ordinary skill in the art, as previously discussed.

The growth substrate containing the substantially perpendicular nanowires was then inverted and slid across a second substrate 20 which contained photoresist 25 thereon, positioned in a predetermined pattern on the second substrate. The photoresist layer, in this example, had a thickness of about 500 nm.

After contact, the first substrate 10 was "slid" over the second substrate 20 (equivalently, the second substrate could have been slid under the first substrate), which allowed at least some of the substantially perpendicular nanowires 15 to be transferred from the first substrate to the second substrate. Due to the motion of the two substrates relative to each other, the nanowires were laid down on the second substrate in substantially the same direction, thereby forming aligned nanowires on the surface of the second substrate (indicated by arrow 17 in Fig. 2). It is believed that the nanowires remained contacted with the second substrate due to van der Waals and similar interactions.

The first substrate was then removed and discarded, leaving behind a series of aligned, substantially oriented nanowires on the surface of the second substrate. The nanowires were present both on the second substrate itself 20, and on the photoresist 25 deposited on top of the second substrate. Optionally, this process can be repeated as desired, e.g., to add additional nanowires to substrate 20 (e.g., nanowires having the same or different composition as nanowires 15, nanowires laid down in a different direction than nanowires 17, etc.).

Next, the photoresist was chemically removed ("lift-off"), e.g., via standard etching processes such as acetone exposure, thereby producing regions that were free of nanowires 22 (corresponding to regions which were previously covered in photoresist 25), as well as regions 21 that contained aligned nanowires (corresponding to regions not previously covered in photoresist 25). Photomicrographs of regions containing aligned nanowires are shown in Figs. 3A and 3B.

Additional circuit elements were next deposited onto the second substrate, for example, to produce a series of thin film transistors or other electrical components, e.g., as is shown in Figs. 4A and 4B. Fig. 4B is an expanded view of one portion of Fig. 4A.

As shown in these figures, transistors were fabricated, each containing gate, drain, and source electrodes (indicated in the photomicrographs by G, D, and S respectively) across channels or regions defined by the aligned, substantially oriented nanowires on the surface of the second substrate ("Ge/Si NW Channels") in Fig. 4A. As discussed below, these components were shown to be functional and reproducible.

EXAMPLE 2

In this example, a series of thin film transistors ("TFT") were prepared on a substrate using the techniques described above in Example 1. 40 separate transistors were prepared in this example using germanium/silicon nanowires having dimensions of approximately 15 nm in diameter and lengths of ~30 micrometers, with a 200 micrometer channel width and a 2 micrometer channel length. The thickness of the gate oxide (tox) was about 12 nm. The characteristics of each of the 40 transistors were individually measured, as is shown in Fig. 5A.

In these experiments, the voltage between the drain and the source (V_{ds}) was held constant at -4 V. The voltage between the gate and the source (V_{gs}) was varied between -6 V and +6 V, and the resulting current (I) was measured. As can be seen in Fig. 5A, the 40 transistors prepared using this method had a fairly narrow distribution, indicating a high degree of reproducibility. These data are summarized in Fig. 5B, which is a histogram plot of the data shown in Fig. 5A. The data in Fig. 5B were determined at a V_{ds} of -4 V and a V_{gs} of -6 V, which was the voltage in Fig. 5A exhibiting the maximum amount of variation. The resulting current was collected in steps of 0.5 mA from -5.5 mA to -2.5 mA. As can be seen, the standard deviation (σ, sigma) of these measurements was roughly 15%.

EXAMPLE 3

This example illustrates the formation of the three-dimensional circuit comprising a plurality of layers of nanowires (or other nanoscale wires). Referring now to Fig. 6, Fig. 6A illustrates a completed device having three layers of aligned nanowires, while Fig. 6B illustrates an example of a technique that was used to produce such a device.

For each layer of nanowires, a growth substrate comprising a plurality of substantially perpendicular nanowires was prepared, and then transferred to a substrate using techniques such as those described in Example 1. In some cases, the substrate may also contain photoresist, which covers various portions of the substrate (see Example 1).

After the deposition of the nanowires onto the substrate and the photoresist (if present), the photoresist may be removed, for example, through standard etching processes.

Next, an additional, intermediate layer of material may be deposited onto the nanowires. The deposited layers may include, for example, additional circuit elements, or an insulating layer. This layer may also contain photoresist, or photoresist may be deposited thereon. A new layer of nanowires can then be deposited on this layer, and the process repeated as many times as desired. As this cyclic process is repeated, multiple layers of the nanowire device may be built up, for example, to produce the final device, such as shown schematically in Fig. 6C.

A photomicrograph of an example of such a multi-layer device, illustrating multiple layers, is shown in Fig. 7, which is an optical image of a 10-layer device. In Fig. 7, each layer is separated by approximately 300 nm of SiO_2 as the intermediate layer of material.

EXAMPLE 4

In this example, the electrical characteristics of a multi-layer device having transistors comprising nanowires is illustrated. This example demonstrates that the characteristics of such electrical components is not substantially affected by the deposition of additional layers on top of the components using the above-described methods.

The multi-layer device was prepared using techniques similar to those described above in Example 3. Geranium/silicon nanowires were used, with a gate oxide HfO_2, deposited using 100 cycles. The nanowires had a diameter of approximately 10 nanometers, and a length of about ~30 micrometers. The channel width and length for the transistors were about 200 micrometers and about 2 micrometers, respectively. For each transistor, the source and the drain electrodes were fabricated from nickel, and the gate electrode was fabricated from aluminum. Between the first layer and the second layer was deposited a 300 nm thick layer of SiO_2 insulation.

Fig. 8 illustrates the transistor characteristics for a transistor on the first layer of a multi-layer device, as deposited, and after a second layer of material had been deposited thereon. The transistor characteristics of a first layer transistor, as fabricated, are shown in solid lines, while the same transistor's characteristics after the additional deposition of a second layer thereon are shown in dotted lines. The transistor characteristics were

measured for various V_{ds} voltages (-1 V, -2 V, -3 V), measured by varying V_{gs} between -6 V and +6 V and measuring the resulting current. As can be seen in Fig. 8, there was no substantial difference in behavior before and after deposition of the second layer onto the transistor.

These experiments can be extended to devices having even greater numbers of layers. For example, in Figs. 9A and 9B, a multi-layer device having 10 layers of germanium/silicon nanowires is illustrated, prepared by repeating the above-described techniques. As can be seen in these figures, there was no substantial difference detected in behavior between transistors deposited in the first layer, in the fifth layer, and in the tenth layer of the multi-layer device. In Fig. 9A, both V_{ds} and V_{gs} were varied (V_{ds} between 0 V and 4 V, V_{gs} in 1.5 V steps), with similar performances for all of the transistors measured on levels 0, 5, and 10 of the device. In Fig. 9B, V_{ds} was held constant at -4 V, while V_{gs} was varied between -6 V and +6 V. Again, similar performances for all of the transistors measured within the multi-layer device.

EXAMPLE 5

This example illustrates that components other than transistors could be successfully prepared within the multi-layer device. In the example, inverters and floating gate memory elements were prepared within a multi-layer device using the techniques described above. The substrate in this example was Kapton-passivated with 2 microns of SU-8, 30 nm of SiO_2 and 500 cycles of HfO_2. The nanowires used in this example were 10 nanometers in diameter, with a length of about ~30 micrometers. The channel width and length for the transistors were about 200 micrometers and about 2 micrometers, respectively. HfO_2 was used at the gate dielectric.

Figs. 10A and 10B show that the inverters prepared in this manner were able to invert an input to a corresponding output. In these figures, the input is shown as channel 1 and the output is shown as channel 2, for various frequencies (50 MHz in Fig. 10A and 95 MHz in Fig. 10B). In both cases, the inverters successfully inverted the input into an output signal.

EXAMPLE 6

This example illustrates the monolithic integration of individual and parallel arrays of crystalline nanowires as multifunctional and multilayer circuits, having up to 10 addressable vertical layers, through a simple "bottom-up" and "top-down" hybrid

methodology. These new assembly-based approaches overcome processing limitations of conventional planar CMOS technology, and thus could make them useful methods for high-performance 3D integrated circuits.

Rational integration of nanowires into functional circuits typically requires that they be assembled with controlled orientation and density at spatially defined locations on the device substrate. Solution-phase methods for assembling aligned and controlled density arrays of nanowires on substrates, including flow-directed and Langmuir-Blodgett techniques, have been reported in U.S. Patent Application Serial No. 09/935,776, filed August 22, 2001, entitled "Doped Elongated Semiconductors, Growing Such Semiconductors, Devices Including Such Semiconductors, and Fabricating Such Devices," by Lieber, *et al.*, published as U.S. Patent Application Publication No. 2002/0130311 on September 19, 2002; U.S. Patent Application Serial No. 10/196,337, filed July 16, 2002, entitled "Nanoscale Wires and Related Devices," by Lieber, *et al.*, published as U.S. Patent Application Publication No. 2003/0089899 on May 15, 2003; U.S. Patent Application Serial No. 10/995,075, filed November 22, 2004, entitled "Nanoscale Arrays, Robust Nanostructures, and Related Devices," by Whang, *et al.*, published as U.S. Patent Application Publication No. 2005/0253137 on November 17, 2005, each incorporated herein by reference.

In this example, a new dry deposition strategy is shown that enables oriented and patterned assembly of nanowires with controlled density and alignment films on substrates, from Si to plastics. The overall process involves (i) optimized growth of designed nanowires by nanocluster directed growth and (ii) patterned transfer of nanowires directly from a nanowire growth substrate to a second device substrate via contact printing, as illustrated in Figure 2. The nanowires were printed by sliding a growth substrate, which included a "lawn" of Ge/Si core/shell nanowires (diameter, ~15 nm; length, ~30 micrometers), against a second device substrate (Si/SiO_2 or Kapton). The Ge/Si nanowires were randomly oriented on the growth substrate, not epitaxial, and were well-aligned by sheer forces during the sliding process. The sliding process resulted in the direct and dry transfer of the nanowires from the growth substrate to the desired device substrate. Prior to transfer, the device substrate was patterned with a photoresist layer (~500 nm thickness). The patterned spacer served to prevent transfer of particles and low-quality nanowire material close to the surface of the growth chip, and

to allow selective assembly of the nanowires at defined locations. After transfer, the patterned photoresist was removed in acetone, leaving the patterned nanowires, which were well-aligned along the sliding direction. Fig. 2 shows contact printing of the nanowires from growth substrate to prepatterned substrate. In general, the nanowires were grown with random (nonepitaxial) orientation and were well-aligned by sheer forces during the printing process.

More specifically, a photolithographically patterned device substrate was first firmly attached to a benchtop, and the nanowire growth substrate was placed upside down on top of the patterned device substrate such that the nanowires were in contact with the device substrate. Gentle manual pressure was then applied from the top followed by sliding the growth substrate 1-3 mm. Finally, the growth substrate was removed. Devices and circuits were then fabricated on the printed arrays of nanowires, using conventional top-down lithography and metallization processes. To elaborate a 3D structure, the nanowire printing and device fabrication steps were iterated multiple times, along with the deposition of an intervening insulating SiO_2 buffer layer, in order to obtain vertically stacked electronic layers (Fig. 6, which shows a three-dimensional nanowire circuit fabricated by the iteration of the contact printing, device fabrication, and separation layer deposition steps *N* times). This process can be used in a wide range of nanowire materials and device designs, as discussed herein, and moreover, the simplicity and the low processing temperature requirement of the method make it very useful for achieving high-performance 3D integrated circuitry with different functionalities in distinct layers.

Single-layer arrays of multi-nanowire FETs (field effect transistors) were fabricated using printed Ge/Si nanowire heterostructures (~10 nm thick core with a ~2 nm shell) as the channel material (Figs. 4A-4B). Fig. 4A is an optical microscope image showing an array of nanowire FETs, while Fig. 4B shows a dark field image demonstrating a parallel array of nanowires aligned between source (S), drain (D), and top gate (G) electrodes. The Ge/Si nanowires, which had higher performance than that of the state-of-the-art planar Si structures, were configured as top-gated devices with channel width and length of 200 micrometers and 2 micrometers, respectively, and a high-κ (kappa) HfO_2 gate dielectric. The FET structures were defined by two photolithography (PL) steps. In the first PL step, the source/drain (S/D) electrodes were

patterned and metallized with Ni (60 nm). A HfO_2 high-κ (kappa) gate dielectric film (thickness, ~12 nm) was deposited by 100 cycles of ALD (atomic layer deposition) at 115 ^{o}C with each cycle having a 1 s water vapor pulse, a 5 s N_2 purge, a 3 s tetrakis(dimethylamino)hafnium [$Hf(N(CH_3)_2)_4$] pulse, and a 5 s N_2 purge. In the second PL step, the top gates were patterned and metallized with Al (60 nm). For multilayer structures, a SiO_2 layer (~300 nm), which serves as a separation layer between active device layers, was deposited by plasma-enhanced CVD or e-beam evaporation. Each additional active nanowire layer was offset in the x and y directions to facilitate imaging and electrical measurements.

Optical microscopy images of the Ge/Si nanwoire FET arrays (Figs. 4A-4B) demonstrate several important features. First, the nanowires were cleanly printed only at lithographically predefined locations on the substrates. Second, the contact printed nanowires were aligned and uniform across millimeter and larger length scales. Third, the nanowires were assembled with relatively high densities (~4 nanowires/micrometer). The local alignment and density was further confirmed by scanning electron microscopy images (Fig. 3A-3B). These features of this methodology thus lead to well-defined and reproducible FET structures over large substrate areas.

The current versus gate-voltage ($I-V_{gs}$) transfer characteristics recorded from an array of 40 Ge/Si FETs fabricated on the same chip is shown in Fig. 5A. Measurements were conducted with a probe station (model 12561B, Cascade Microtech) and a semiconductor parameter analyzer (model 4156C, Agilent). For AC characterization of the inverters, a function generator (model 8648B, Agilent) was used to provide high-frequency voltage pulses for the input, while the output voltage was monitored by an oscilloscope (model TDS3012, Tektronix) using a high-impedance FET probe (model 12C, Picoprobe).

Notably, as shown in Fig. 5A, the FETs showed minimal variation in the threshold voltage and exhibited a large average on-current of 4 mA with a 1-standard deviation variation of only 15%. This may be due to good device-to-device reproducibility to the uniformity of the contact printed Ge/Si nanowires and/or averaging of nanowire-to- nanowire variations within the multi-nanowire device. Reproducible behavior is, of course, important for nanomaterial building blocks in integrated circuits and other applications. To achieve reliable 3D integration of this particular device, it is

also important that layer-by-layer assembly and fabrication process does not alter the electrical properties of previous layers. Fig. 8 shows the transfer characteristics of a first-layer FET with a multi-nanowire channel, before and after the vertical stacking of the second layer, where the I-V_{gs} data showed no significant change of the on current. These results demonstrate that the assembly and fabrication steps involved in adding layers have little or no effect on the device properties. Thus, this methodology may be compatible with monolithic 3D integration of various nanowire electronic layers on a single chip.

To illustrate 3D integration, a structure was assembled and fabricated that had 10 layers of Ge/Si multi-nanowire FETs on a Si substrate, as shown in Fig. 7 (optical microscope image). The optical image shows the source, drain, gate electrode structure of FETs in each of the 10 layers, which were offset in x and y between layers for clarity. Optical interference further lead to distinct colors in the upper layers. In addition, the current versus drain source voltage (I-V_{ds}) output characteristics (with a 1.5 V gate step) of the nanowire FETs in layers 1, 5, and 10 for the assembled 3D structure were characterized, as shown in Figs. 9A and 9B. Notably, the 3D nanowire FET structure exhibited consistent layer-to-layer electrical properties with on-currents of about 3 mA and a maximum transconductance, gm, of about 1 mS. These data demonstrate the reproducibility and reliability of this assembly and fabrication process for individual device layers, and the ability to vertically stack these layers without performance degradation.

Thus, the 10-layer nanowire 3D electronic structure shows a highest number of functional device layers, using single-crystalline channel materials that have been vertically stacked. In planar Si technology, it has been difficult to achieve true 3D integrated structures, due in part to materials-related challenges associated with high-temperature processing needed to produce single-crystalline silicon. This approach represents a unique opportunity for high-performance 3D integrated circuitry, owing to fact that higher temperature materials growth, which enables single-crystalline functional nanowires, is independent of the low processing assembly and fabrication steps used to complete each layer.

EXAMPLE 7

One advantage of the approach discussed in Example 6 is that the on-current can be readily scaled simply by adjusting the device width and nanowire density in order to meet the specific circuit needs. To demonstrate this capability, in this example, vertically stacked layers of FETs based on only single Ge/Si nanowires were fabricated. Low Ge/Si nanowire density growth substrates were used for the contact printing step in order to reduce the density of transferred nanowires, while much narrower 1 micrometer width S/D electrodes were used to ensure a high yield of single-nanowire devices.

An optical microscopy image of a five-layer structure, including single nanowire FETs with multiple sources and a common drain with a top gate, is shown in Fig. 11A, together with a schematic of an addressable single-nanowire device structure. The low-resolution image (Fig. 11A, left) shows the nanowire FETs in successive layers, where the FET arrays in each layer are offset in x and y for clarity. In addition, high-resolution images (Fig. 11A, middle) demonstrate that the desired single-nanowire top-gated FET devices were formed in the five-layer structure.

The electrical properties of representative devices from layers 1 and 5 are shown in Figs. 11B and 11C. Fig. 11B shows I-V_{ds} (with 1 V gate step) of single-nanowire FETs on layers 1 and 5, while Fig. 11C shows I-V_{gs} for single-nanowire devices on layers 1 and 5. Good reproducibility was observed in the FET properties from lower (layer 1) and upper (layer 5) FETs even for these single-nanowire devices. The Ge/Si FETs delivered on currents, I_{ON}, of ~10 microamperes at V_{ds} = 1 V with gm of 7 microsiemens. Scaled Ge/Si nanowire FETs may afford diameter-normalized I_{ON} and gm values of 2.1 mA/micrometers and 3.3 mS/micrometers, respectively, both of which are better than state-of-the-art planar Si technology. Hence, coupling this 3D methodology with Ge/Si nanowires building blocks and advanced lithography (to produce small channels) can lead to ultrahigh-performance 3D electronics not accessible by scaled CMOS.

EXAMPLE 8

This example illustrates the assembly and fabrication of multifunctional 3D nanowire electronics on flexible substrates utilizing techniques similar to those described above. As shown schematically in Fig. 12A, the 3D structure used in this example included a lower layer of PMOS inverters and an upper layer of floating gate memory elements. The inverter-memory structures were assembled on plastic substrates, which

were chosen to illustrate further the versatility of this approach, using Ge/Si nanowires as the active semiconductor material. More specifically, the multifunctional layers of the PMOS inverters (layer 1) and the floating gate memory (layer 2) were fabricated on a Kapton polyimide substrate (DuPont). The inverter structures included nickel S/D (60 nm) and titanium top gate (60 nm) with HfO_2 (~20 nm) as a gate dielectric. For the floating gate memory, nickel was used for the S/D (60 nm), floating gate (30 nm), and control gate (30 nm). An approximately 9 nm thick HfO_2 layer was used as the tunnel oxide, while an approximately 20 nm HfO_2 layer was used as the intergate oxide. An optical image of a typical 3D structure (Fig. 12B) shows the lower inverter logic layer (layer 1) and offset in the x upper memory layer (layer 2) on Kapton. Each inverter logic gate included a load and a switching FET, and the memory devices included an FET with a floating gate separated from the nanowire channel by a thin tunnel oxide and from the control gate by a thicker oxide.

The electrical characteristics of the multifunctional device structure were characterized in several ways. First, output (V_{out}) versus input (V_{in}) behavior (Fig. 12C) showed well-defined inversion with quasi-DC gain of 3.5. The inset shows functional devices on flexible Kapton substrate. Second, frequency-dependent measurements (Fig. 12D) demonstrated that the gain was greater than unity and phase inversion was achieved when the devices were driven by up to a 50 MHz sine wave at a supply voltage of 4 V. This is higher than other operation frequencies for a circuit made of any channel material on flexible substrates, outperforming amorphous Si and organic electronics by over 2 orders of magnitude. The nanowire inverter structure can be further improved to obtain higher frequencies by using shorter channel lengths and incorporating thinner gate dielectrics. Third, current vs. voltage sweeps recorded on the memory elements (Fig. 13A) exhibited large and reproducible hysteresis loops of storage and removal of charge from a floating gate element. Fourth, to further elucidate the properties of the nanowire memory devices, writing and erasing operations were carried out by applying short, 1 ms pulses of $\pm$15 V to the control gate. As shown in Fig. 13B, these pulses resulted in well-defined and nonvolatile ON and OFF states transitions, while the control gate is maintained at V_{CG} = 5 V during the reading phase (Fig. 13B). Further device optimization can lower the operating voltage of the nanowire memory devices by scaling the oxide layers and also incorporating oxide engineering.

EXAMPLE 9

This example illustrates the interconnection of nanowire FETs, including vertical scaling. A nanowire FET device was prepared using techniques similar to those described above. Fig. 14A is an optical microscope image of an interconnected two-layer PMOS FETs. Fig. 14B shows the transfer characteristics of nanowire FETs, before and after interconnection. It can be seen that the on-current within the FETs can be increased by multiple times after interconnection, as measured by I_{ds}:

	On current (microamps)	Transconductance (microsiemens)
1st layer	238	89
2nd layer	231	79
Interconnect	475	139

Similar results can be seen with respect to interconnected PMOS nanowire inverters. For example, Fig. 15C illustrates the DC characteristics of a PMOS nanowire inverter, while Fig. 15D illustartes the AC characteristics of the inverter. The interconnected PMOs inverter discussed here shows a quasi-DC gain of about 5 and a unity voltage gain frequency of about 20 MHz at a supply voltage (V_{DD}) of about 4V. The device itself can be seen in Figs. 15A and 15B. Fig. 15B shows the distribution of components within the device. Fig. 15A is a photomicrograph of the device.

EXAMPLE 10

A nanoscale ring oscillator was prepared as is shown in Figs. 16A-16D. Fig. 16A shows a circuit schematic diagram of the ring oscillator structure, including the distribution of components within 2 layers of a device, produced using techniques similar to those described above. The ring oscillator was fabricated using Ge/Si core /shell (p-type) nanowire FETs. Microscopy images of the ring oscillator structure can be seen in Figs. 16B and 16C. Fig. 16D illustrates a cross-sectional schematic diagram of a portion of the nanowire ring oscillator. Electrical characteristics of this device can be seen in Figs. 16E and 16F. Fig. 16E shows an oscillation frequency for the device, of about 6.3 MHz. The oscillation frequency was found to be a function of supply voltage (V_{DD}), as is shown in Fig. 16F. Thus, the interconnected PMOS ring oscillator demonstrated here produced a stable output frequency of about 6.3 MHz and a 1.5 V output voltage swing.

EXAMPLE 11

This example illustrates an interconnected CMOS nanowire inverter. Fig. 17A shows a schematic diagram of the nanowire inverter, including the distribution of components within 2 layers of a device, produced using techniqeus similar to the above-described ones. The interconnected CMOS nanowire inverters were fabricated with the first layer being NMOS FET (InAs nanowires), and the second layer being PMOS FET (Ge/Si nanowires). Figs. 17B and 17C illustrate photomicrographs of the device. Electrical characteristics of this device can be seen in Figs.17D and 17E. Fig. 17D shows that the interconnected CMOs inverter had a quasi-DC gain of 15 and a unity voltage gain frequency of about 50 MHz at a supply voltage (V_{DD}) of 4 V. Fig. 17E shows the unity voltage gain frequency (about 50 MHz) of the device.

EXAMPLE 12

In this example, an interconnected CMOS nanowire ring oscillator is demonstrated. Fig. 18A shows a circuit schematic diagram of the CMOS ring oscillator, including the distribution of components within 2 layers of a device, using techniques similar to those described above. The ring oscillators were fabricated with complementary InAs (n-type, 1st layer) and Ge/Si (p-type, 2nd layer) nanowires. Photomicrographs of the device are shown in Figs. 18B and 18C. Electrical characterization of this device can be seen in Fig. 18D, showing an oscillation frequency of 13.9 MHz at a V_{DD} of 5 V and a 2 V output voltage swing. The supply voltage was also found to be lower compared to other PMOS ring oscillators.

While several embodiments of the present invention have been described and illustrated herein, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the functions and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the present invention. More generally, those skilled in the art will readily appreciate that all parameters, dimensions, materials, and configurations described herein are meant to be exemplary and that the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the teachings of the present invention is/are used. Those skilled in the art will recognize, or be able to ascertain using no more than routine

experimentation, many equivalents to the specific embodiments of the invention described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, the invention may be practiced otherwise than as specifically described and claimed. The present invention is directed to each individual feature, system, article, material, kit, and/or method described herein. In addition, any combination of two or more such features, systems, articles, materials, kits, and/or methods, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the scope of the present invention.

All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

The indefinite articles "a" and "an," as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean "at least one."

The phrase "and/or," as used herein in the specification and in the claims, should be understood to mean "either or both" of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with "and/or" should be construed in the same fashion, i.e., "one or more" of the elements so conjoined. Other elements may optionally be present other than the elements specifically identified by the "and/or" clause, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to "A and/or B", when used in conjunction with open-ended language such as "comprising" can refer, in one embodiment, to A only (optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

As used herein in the specification and in the claims, "or" should be understood to have the same meaning as "and/or" as defined above. For example, when separating items in a list, "or" or "and/or" shall be interpreted as being inclusive, i.e., the inclusion of at least one, but also including more than one, of a number or list of elements, and, optionally, additional unlisted items. Only terms clearly indicated to the contrary, such

as "only one of" or "exactly one of," or, when used in the claims, "consisting of," will refer to the inclusion of exactly one element of a number or list of elements. In general, the term "or" as used herein shall only be interpreted as indicating exclusive alternatives (i.e. "one or the other but not both") when preceded by terms of exclusivity, such as "either," "one of," "only one of," or "exactly one of." "Consisting essentially of," when used in the claims, shall have its ordinary meaning as used in the field of patent law.

As used herein in the specification and in the claims, the phrase "at least one," in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, "at least one of A and B" (or, equivalently, "at least one of A or B," or, equivalently "at least one of A and/or B") can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

It should also be understood that, unless clearly indicated to the contrary, in any methods claimed herein that include more than one step or act, the order of the steps or acts of the method is not necessarily limited to the order in which the steps or acts of the method are recited.

In the claims, as well as in the specification above, all transitional phrases such as "comprising," "including," "carrying," "having," "containing," "involving," "holding," "composed of," and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases "consisting of" and "consisting essentially of" shall be closed or semi-closed transitional phrases,

respectively, as set forth in the United States Patent Office Manual of Patent Examining Procedures, Section 2111.03.

What is claimed is:

CLAIMS

1. A method, comprising:

providing a first substrate having a plurality of nanoscale wires thereon;

contacting at least some of the plurality of nanoscale wires with a second substrate; and

transferring at least some of the plurality of nanoscale wires from the first substrate to the second substrate.

2. The method of claim 1, wherein at least some of the plurality of nanoscale wires on the first substrate are attached to a surface of the first substrate via respective points of attachment.

3. The method of claim 2, wherein at least some of the plurality of nanoscale wires on the first substrate are substantially perpendicular to the surface of the first substrate prior to contacting with the second substrate.

4. A method, comprising:

providing a first substrate having a plurality of nanoscale wires attached to a surface of the substrate via respective points of attachment;

contacting at least some of the plurality of nanoscale wires with a second substrate; and

moving at least one of the first and second substrates such that at least some of the plurality of nanoscale wires are moved into an orientation substantially parallel to the surface of the first substrate.

5. The method of claim 4, wherein the plurality of nanoscale wires are substantially perpendicular to the surface of the first substrate prior to contacting with the second substrate.

6. The method of claim 4, further comprising transferring at least some of the plurality of nanoscale wires from the first substrate to the second substrate.

7. A method, comprising:

providing a substrate having a plurality of nanoscale wires attached to a surface of the substrate via respective points of attachment; and

applying a force to at least some of the plurality of nanoscale wires such that at least some of the plurality of nanoscale wires are moved into an orientation substantially parallel to the surface of the substrate.

8. The method of claim 7, wherein at least some of the plurality of nanoscale wires on the substrate are substantially perpendicular to the surface of the first substrate prior to applying the force.

9. The method of claim 7, wherein the force is applied to the plurality of nanoscale wires via a second substrate.

10. A method, comprising:

providing a first substrate having a plurality of nanoscale wires attached to a surface of the first substrate via respective points of attachment;

providing a second substrate spaced a distance away from the first substrate, the second substrate substantially parallel to the first substrate, such that at least one nanoscale wire attached to the first substrate is in physical contact with the second substrate; and

decreasing the spacing between the first substrate and the second substrate such that the first substrate and the second substrate remain substantially parallel.

11. The method of claim 10, wherein the plurality of nanoscale wires are attached to a surface of the first substrate via respective points of attachment.

12. The method of claim 10, wherein the plurality of nanoscale wires are substantially perpendicular to the surface of the first substrate.

13. The method of claim 10, wherein the spacing is decreased such that the spacing is less than the average length of the plurality of nanoscale wires.

14. The method of claim 10, wherein the spacing is decreased such that the spacing is less than half the average length of the plurality of nanoscale wires.

15. The method of claim 10, further comprising transferring at least some of the plurality of nanoscale wires from the first substrate to the second substrate.

16. A method, comprising:

aligning a plurality of nanoscale wires substantially parallel relative each other on a surface of a substrate without exposing the plurality of nanoscale wires to a liquid.

17. The method of claim 16, wherein at least some of the plurality of nanoscale wires on the substrate are attached to the surface via respective points of attachment.

18. The method of claim 17, wherein at least some of the plurality of nanoscale wires are substantially perpendicular to the surface of the substrate.

19. The method of claim 16, wherein the substrate comprises a polymer.

20. The method of claim 16, wherein the substrate degrades at a temperature greater than about 500 °C.

21. The method of any one of claims 1, 4, 7, 10, or 16, further comprising depositing a layer of material on the plurality of nanoscale wires.

22. The method of claim 21, wherein the layer of material comprises photoresist.

23. The method of claim 21, further comprising depositing a second plurality of nanoscale wires on the layer of material.

24. The method of any one of claims 1, 4, 7, 10, or 16, further comprising immobilizing a reaction entity with respect to at least some of the plurality of nanoscale wires.

25. The method of any one of claims 1, 4, 7, 10, or 16, wherein at least some of the plurality of nanoscale wires are nanotubes.

26. The method of any one of claims 1, 4, 7, 10, or 16, wherein at least some of the plurality of nanoscale wires are nanowires.

27. The method of any one of claims 1, 4, 7, 10, or 16, wherein at least some of the plurality of nanoscale wires are semiconductor nanowires.

28. The method of any one of claims 1, 4, 7, 10, or 16, wherein the plurality of nanoscale wires each has substantially the same composition.

29. The method of any one of claims 1, 4, 7, 10, or 16, wherein the plurality of nanoscale wires has an average diameter of less than about 500 nm.

30. The method of any one of claims 1, 4, 7, 10, or 16, wherein the plurality of nanoscale wires are substantially straight.

31. The method of any one of claims 1, 4, 7, 10, or 16, wherein the plurality of nanoscale wires are substantially rigid.

32. The method of any one of claims 1, 4, 7, or 10, wherein the plurality of nanoscale wires is not exposed to a liquid.

33. The method of any one of claims 1, 4, or 10, wherein the plurality of nanoscale wires on the first substrate has a density of at least about 100 nanoscale wires/micrometer^2.

34. The method of any one of claims 7 or 16, wherein the plurality of nanoscale wires on the substrate has a density of at least about 100 nanoscale wires/micrometer^2.

35. The method of any one of claims 1, 4, or 10, further comprising discarding the first substrate.

36. The method of any one of claims 1, 4, or 10, wherein the first substrate comprises a semiconductor material.

37. The method of any one of claims 1, 4, or 10, wherein the second substrate comprises a semiconductor material.

38. The method of any one of claims 1, 4, or 10, wherein the second substrate comprises a polymer.

39. The method of any one of claims 1, 4, or 10, wherein the second substrate degrades at a temperature greater than about 500 °C.

40. The method of any one of claims 7 or 16, wherein the substrate comprises a semiconductor material.

41. The method of any one of claims 1, 4, or 10, wherein the second substrate is not flat.

42. The method of any one of claims 1, 4, or 10, wherein the second substrate comprises at least a first region at a first height, and a second region at a second height different from the first height.

43. The method of any one of claims 1, 4, or 10, wherein the second substrate comprises a region comprising an additional material thereon.

44. An article, comprising:

a first substrate;

a second substrate substantially parallel to the first substrate; and

a plurality of nanoscale wires, at least some of which each has a first end in contact with the first substrate and a second end in contact with the second substrate not immobilized relative to the first substrate.

45. The article of claim 44, wherein the plurality of nanoscale wires are substantially perpendicular to the surface of the first substrate.

46. The article of claim 44, wherein the second substrate is spaced a distance away from the first substrate such that the spacing is less than the average length of the plurality of nanoscale wires.

47. The article of claim 46, wherein the spacing is less than half the average length of the plurality of nanoscale wires.

48. The article of claim 44, wherein the plurality of nanoscale wires on the first substrate has a density of at least about 100 nanoscale wires/micrometer^2.

49. The article of claim 44, wherein the first substrate comprises a semiconductor material.

50. The article of claim 44, wherein the second substrate comprises a semiconductor material.

51. The article of claim 44, wherein the second substrate comprises a polymer.

52. The article of claim 44, wherein the second substrate degrades at a temperature greater than about 500 °C.

53. An article, comprising:

a first plurality of nanoscale wires intersected by a first plane;

a second plurality of nanoscale wires intersected by a second plane; and

an intermediate layer of non-fluid material positioned between the first plane of nanoscale wires and the second plane of nanoscale wires.

54. The article of claim 53, wherein the first plurality of nanoscale wires are substantially aligned in parallel relative to each other.

55. The article of claim 54, wherein the second plurality of nanoscale wires are substantially aligned in parallel relative to each other.

56. The article of claim 55, wherein each of the first and the second pluralities of nanoscale wires are substantially aligned in a common direction.

57. The article of claim 53, wherein at least a portion of the first plurality of nanoscale wires is in electrical communication with at least a portion of the second plurality of nanoscale wires.

58. The article of claim 53, wherein the first plane and the second plane are substantially parallel.

59. The article of claim 53, wherein the intermediate layer comprises photoresist.

60. The article of claim 53, further comprising:

a third plurality of nanoscale wires intersected by a third plane; and

a second intermediate layer of non-fluid material positioned between the second plane of nanoscale wires and the third plane of nanoscale wires.

61. The article of claim 60, further comprising:

a fourth plurality of nanoscale wires intersected by a fourth plane; and

a third intermediate layer of non-fluid material positioned between the third plane of nanoscale wires and the fourth plane of nanoscale wires.

62. The article of claim 61, further comprising:

a fifth plurality of nanoscale wires intersected by a fifth plane; and

a fourth intermediate layer of non-fluid material positioned between the fourth plane of nanoscale wires and the fifth plane of nanoscale wires.

63. The article of claim 53, wherein at least some of the first plurality of nanoscale wires are nanotubes.

64. The article of claim 53, wherein at least some of the first plurality of nanoscale wires are nanowires.

65. The article of claim 53, wherein at least some of the first plurality of nanoscale wires are semiconductor nanowires.

66. The article of claim 53, wherein the first plurality of nanoscale wires each has substantially the same composition.

67. The article of claim 53, wherein the first plurality of nanoscale wires has an average diameter of less than about 500 nm.

68. An article, comprising:

a unitary device comprising at least 5 planar layers of circuitry.

69. The article of claim 68, wherein at least one of the planar layers comprises a nanoscale wire.

70. The article of claim 68, wherein each of the planar layers comprises nanoscale wires.

71. The article of claim 68, wherein the unitary device further comprises an intermediate layer of non-fluid material positioned between at least two planar layers of circuitry.

72 The article of claim 71, wherein the intermediate layer of non-fluid material comprises photoresist.

73. A method, comprising:

providing a substrate comprising a first layer of nanoscale wires;

depositing an intermediate layer of non-fluid material on the first layer of nanoscale wires; and

depositing a second layer of nanoscale wires on the intermediate layer of non-fluid material.

74. The method of claim 73, wherein the first layer comprises nanoscale wires substantially aligned in parallel relative to each other.

75. The method of claim 73, further comprising depositing a second intermediate layer of non-fluid material on the second layer of nanoscale wires.

76. The method of claim 75, further comprising depositing a third layer of nanoscale wires on the second intermediate layer of non-fluid material.

77. The method of claim 76, further comprising:

depositing a third intermediate layer of non-fluid material on the third layer of nanoscale wires; and

depositing a fourth layer of nanoscale wires on the third intermediate layer of non-fluid material.

78. The method of claim 77, further comprising:

depositing a fourth intermediate layer of non-fluid material on the fourth layer of nanoscale wires; and

depositing a fifth layer of nanoscale wires on the fourth intermediate layer of non-fluid material.

79. A method, comprising:

providing a substrate comprising a first layer of nanoscale wires, at least some of which are substantially parallel; and

depositing, with respect to the substrate, a second layer of nanoscale wires, at least some of which are substantially parallel to the first substantially parallel nanoscale wires.

80. The method of claim 79, further comprising depositing, with respect to the substrate, a third layer of nanoscale wires, at least some of which are substantially parallel to the first substantially parallel nanoscale wires.

81. The method of claim 80, further comprising depositing, with respect to the substrate, a fourth layer of nanoscale wires, at least some of which are substantially parallel to the first substantially parallel nanoscale wires.

82. The method of claim 81, further comprising depositing, with respect to the substrate, a fifth layer of nanoscale wires, at least some of which are substantially parallel to the first substantially parallel nanoscale wires.

83. A method, comprising:

forming an electronic circuit comprising nanoscale wires, substantially aligned in parallel relative to each other, disposed on a photoresist.

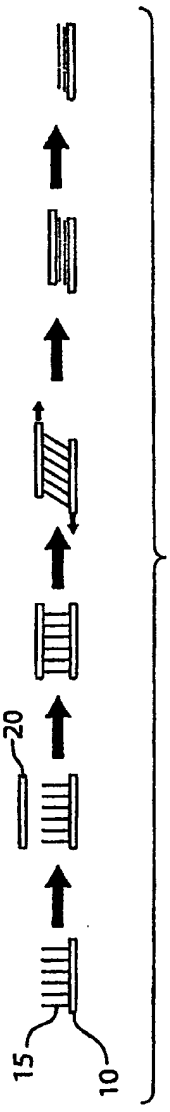


Fig. 1A

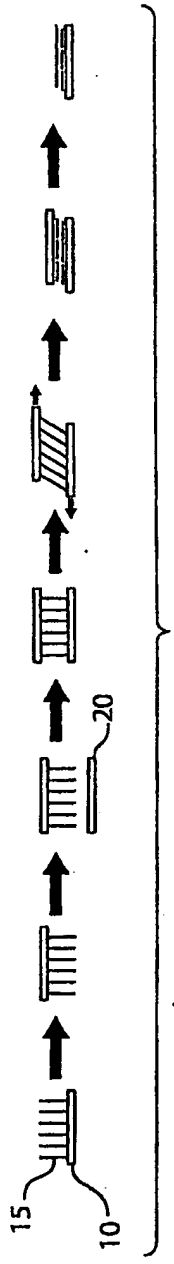


Fig. 1B

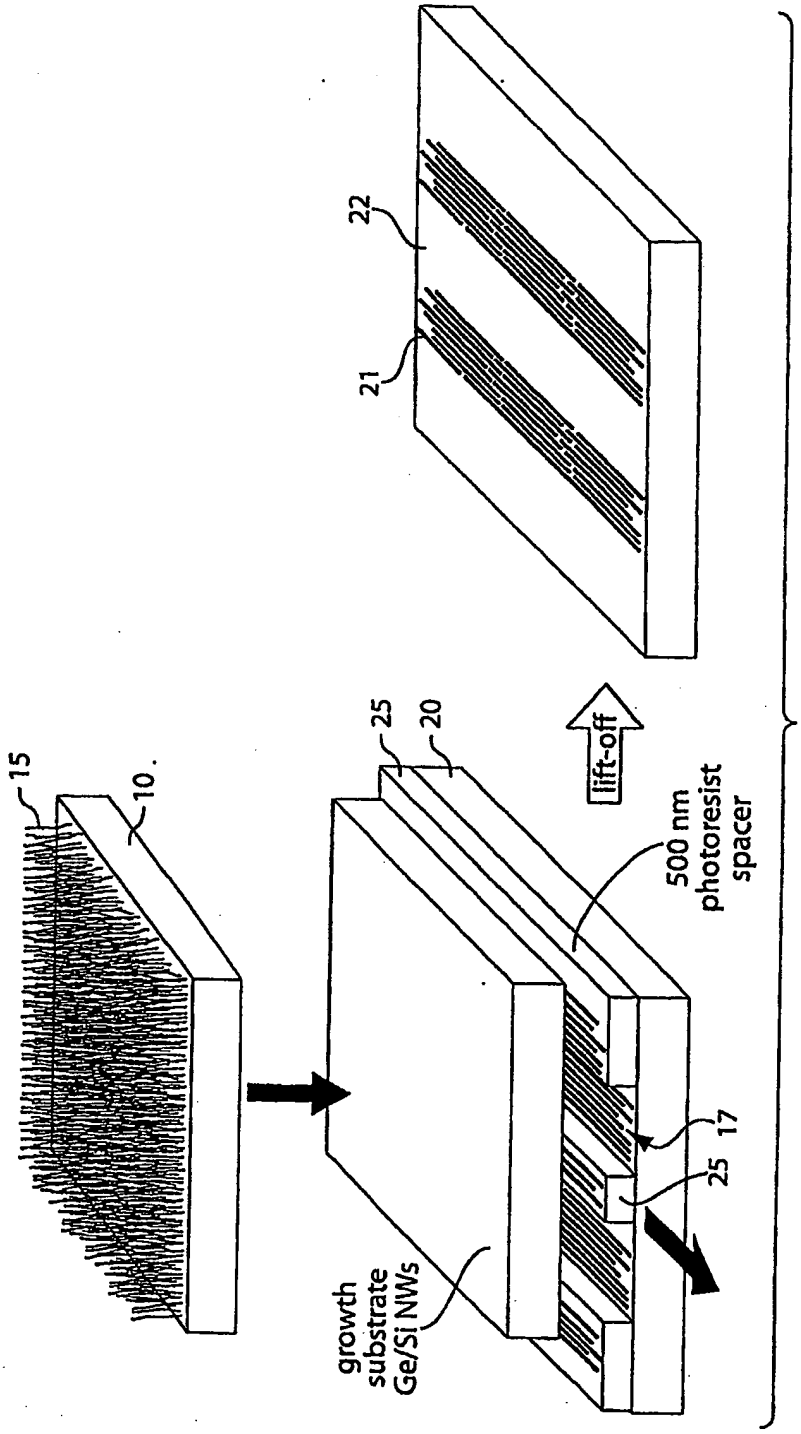

22
21
lift-off
25
20
15
10
500 nm
photoresist
spacer
17
25
growth
substrate
Ge/Si NWs

Fig. 2

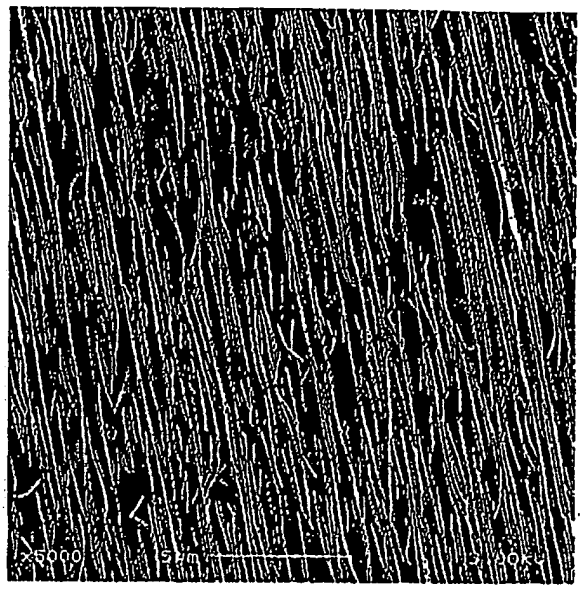


Fig. 3A

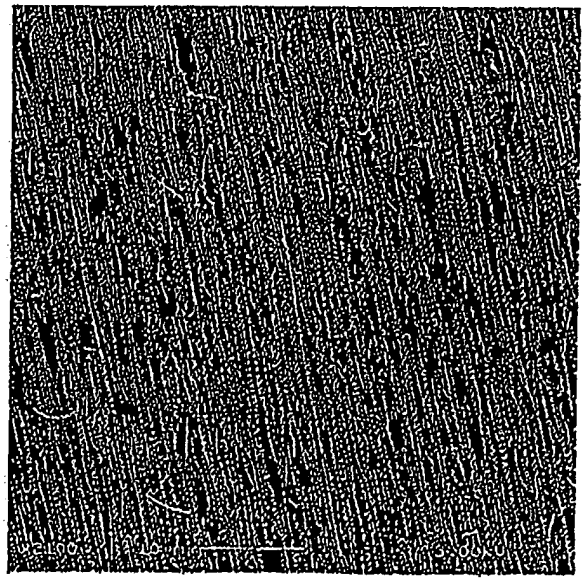


Fig. 3B

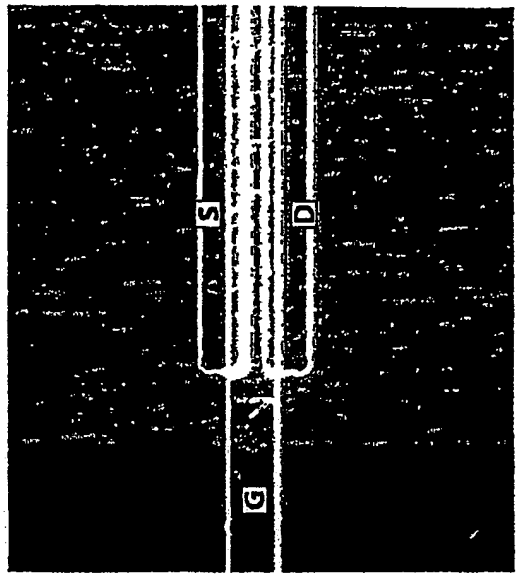


Fig. 4B

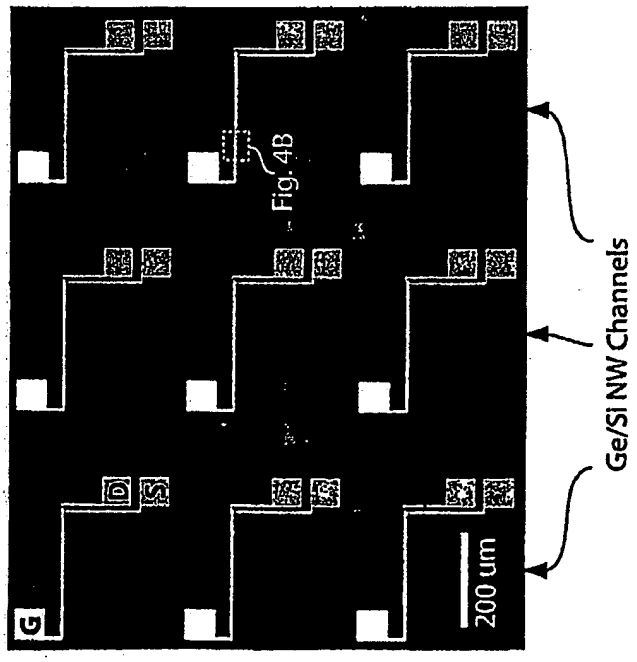


Fig. 4A

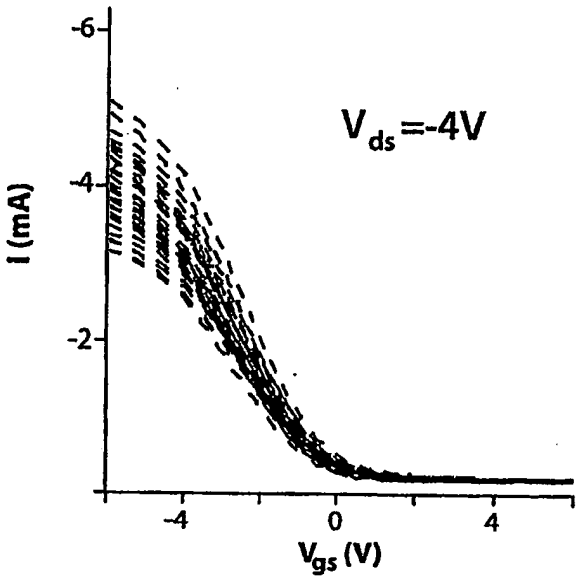

-6
-4
-2
I (mA)
V_{ds}=-4V
-4
0
4
V_{gs} (V)

Fig. 5A

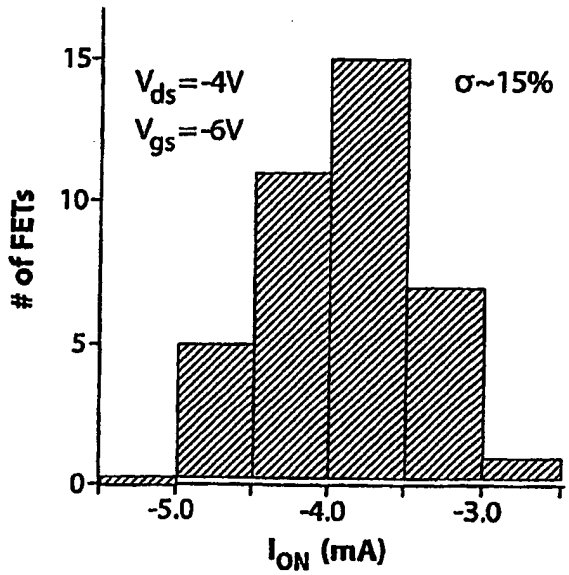

15
10
5
0
# of FETs
V_{ds}=-4V
V_{gs}=-6V
σ~15%
-5.0
-4.0
-3.0
I_{ON} (mA)

Fig. 5B

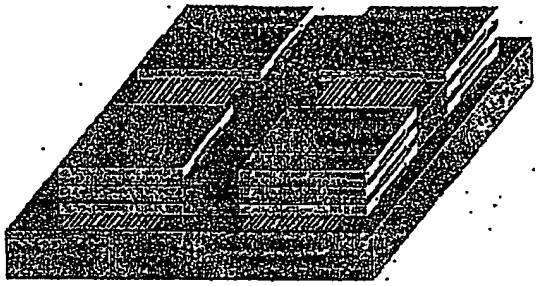


Fig. 6A

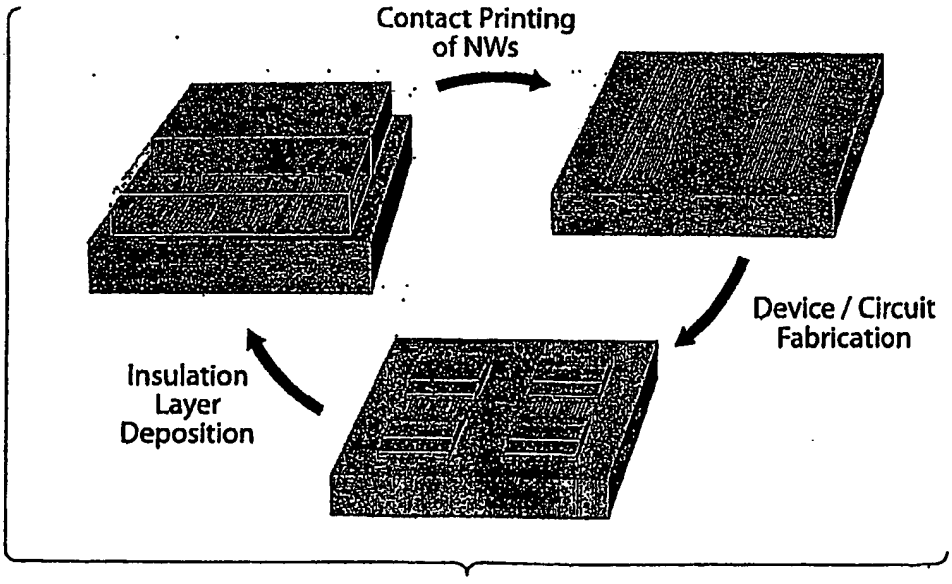

Contact Printing
of NWs
Device / Circuit
Fabrication
Insulation
Layer
Deposition

Fig. 6B

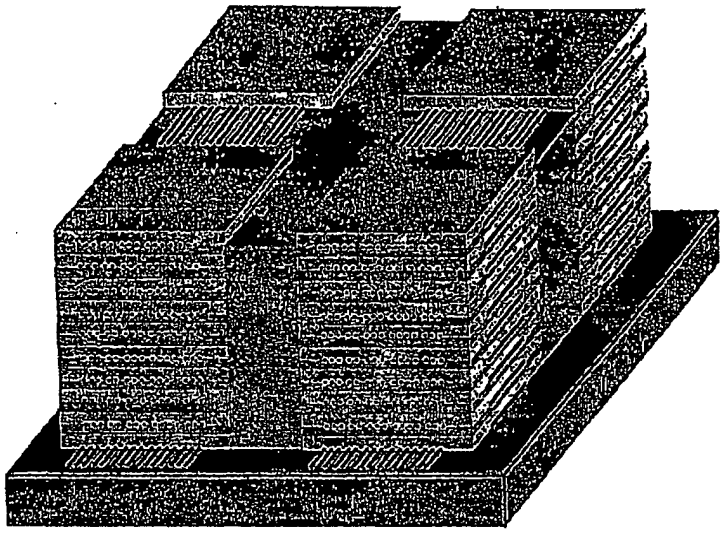


Fig. 6C

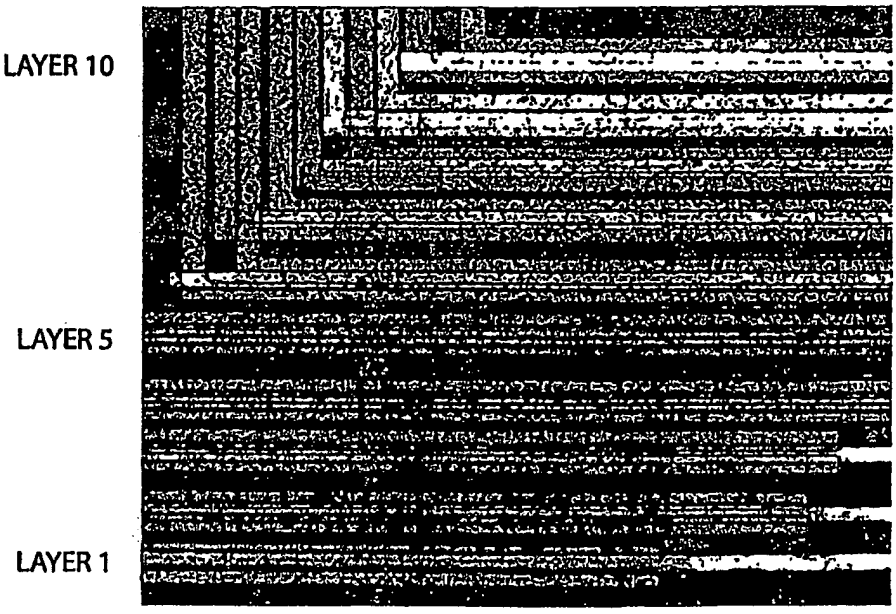


Fig. 7

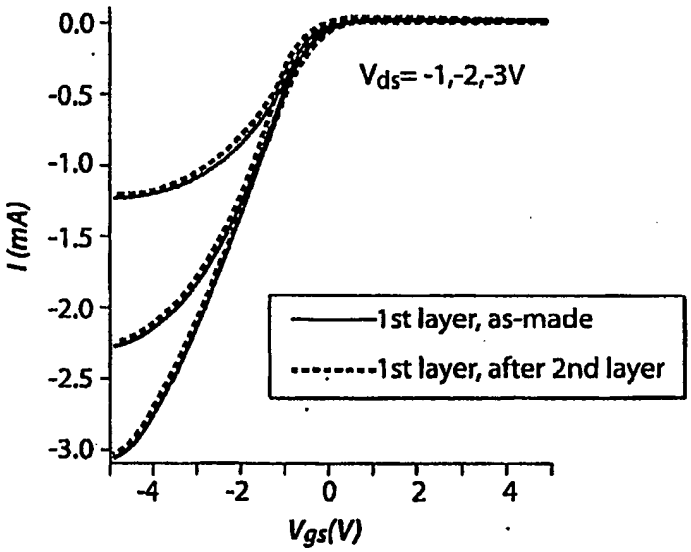

0.0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
I (mA)
-4
-2
0
2
4
Vgs(V)
Vds= -1,-2,-3V
1st layer, as-made
1st layer, after 2nd layer

Fig. 8

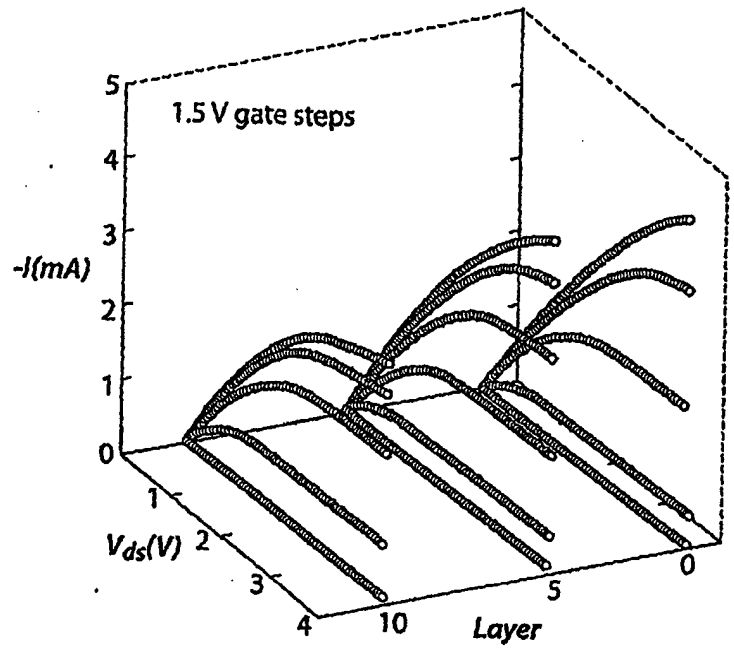

1.5 V gate steps
-I(mA)
5
4
3
2
1
0
1
2
3
4
V_{ds}(V)
10
5
0
Layer

Fig. 9A

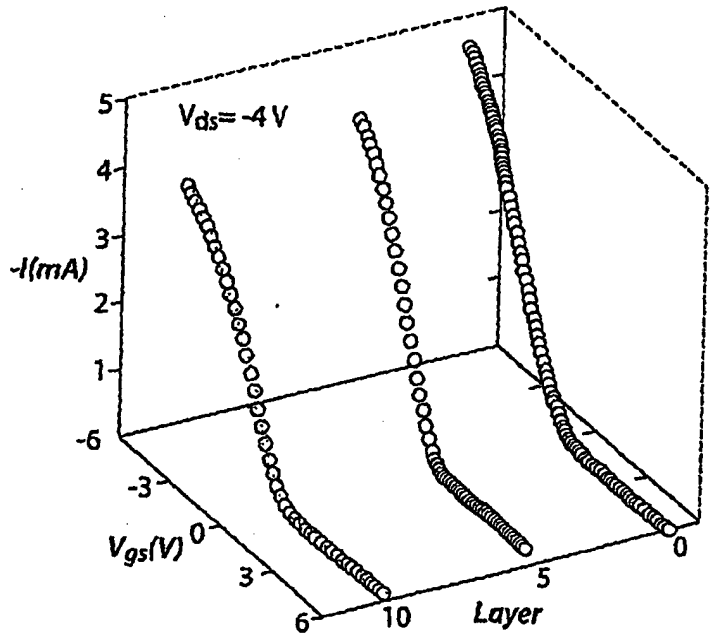

V_{ds}= -4 V
-I(mA)
5
4
3
2
1
-6
-3
0
3
6
V_{gs}(V)
10
5
0
Layer

Fig. 9B

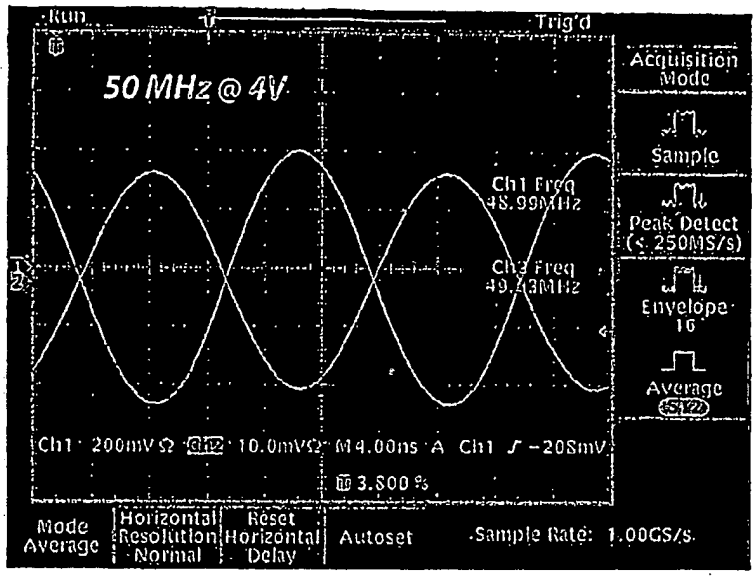


Fig. 10A

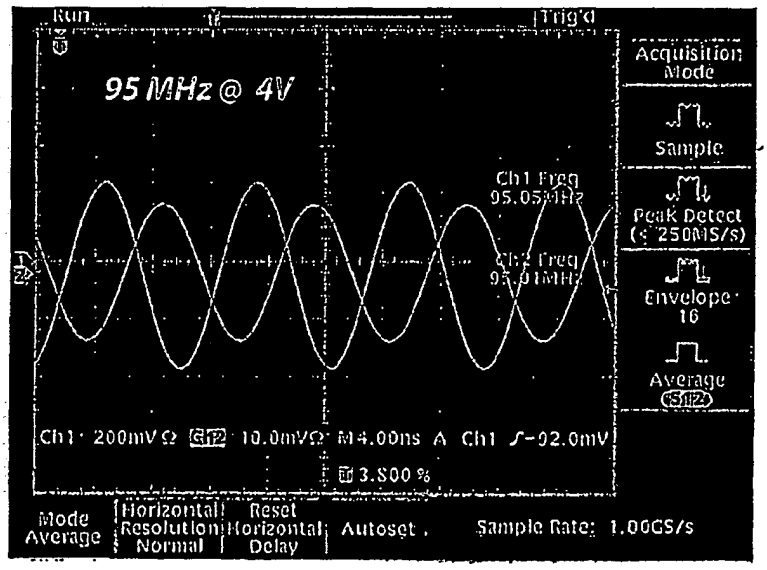


Fig. 10B

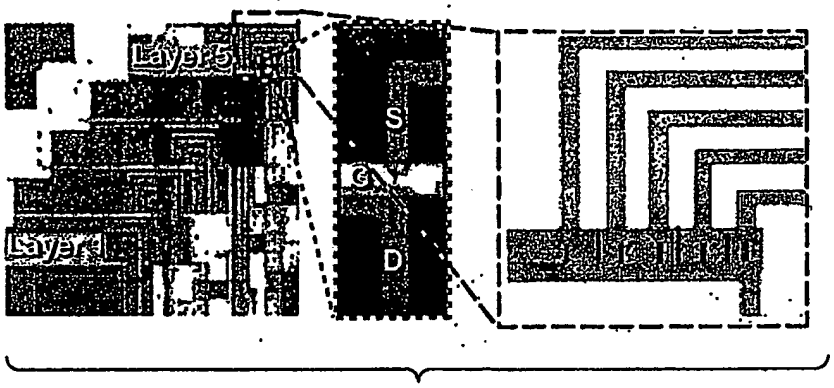


Fig. 11A

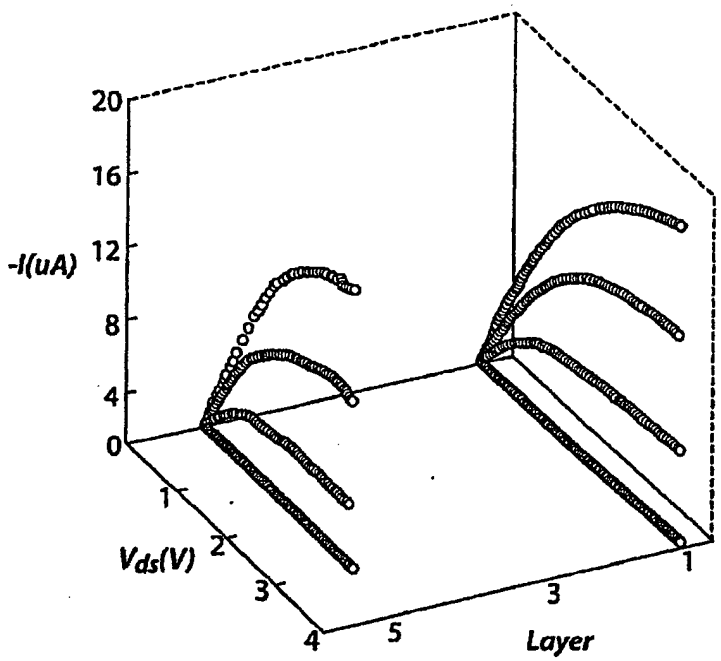


Fig. 11B

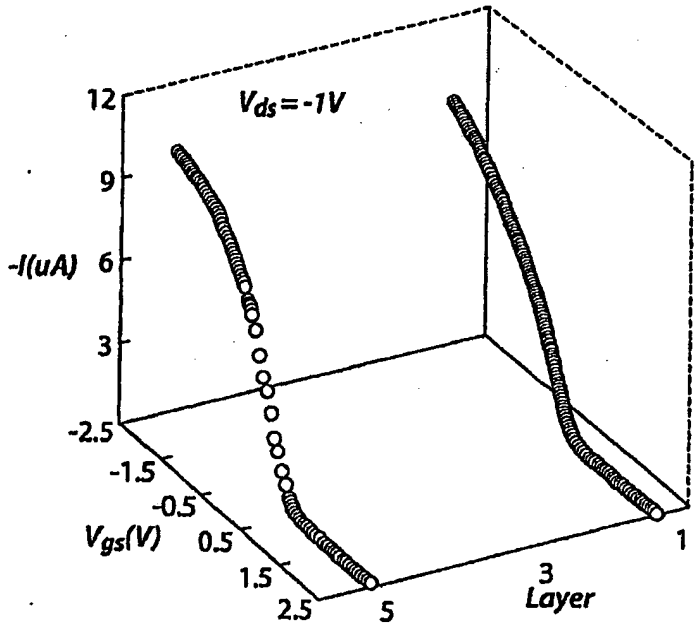


Fig. 11C

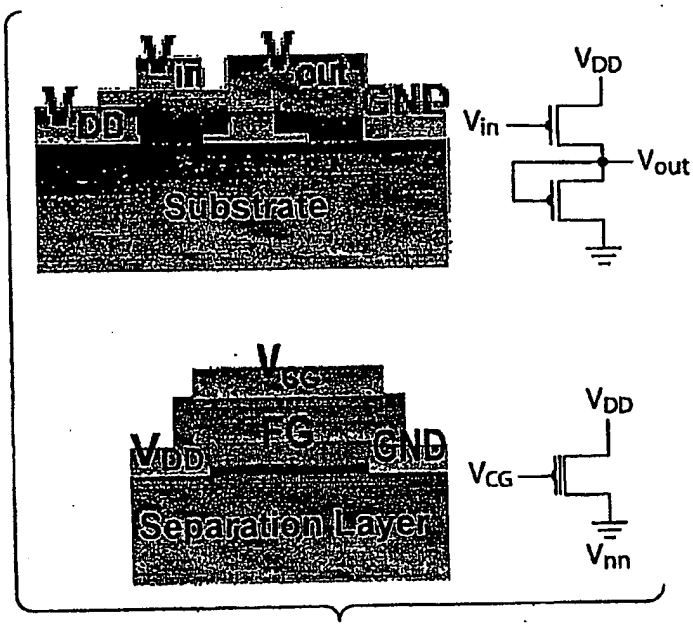


Fig. 12A

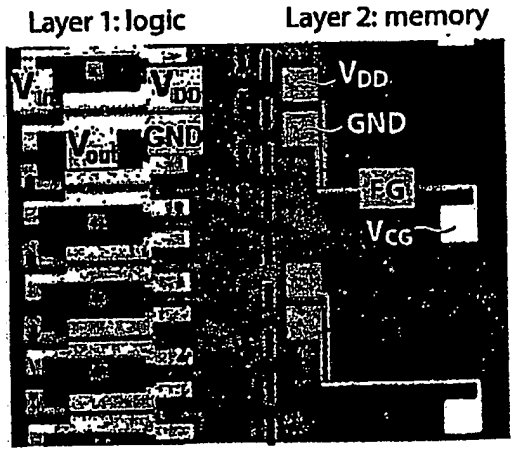


Fig. 12B

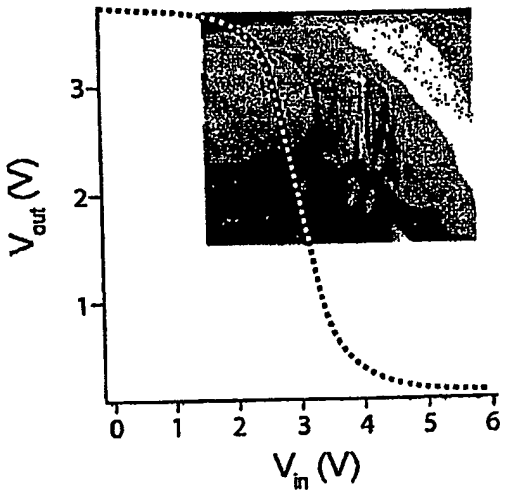


Fig. 12C

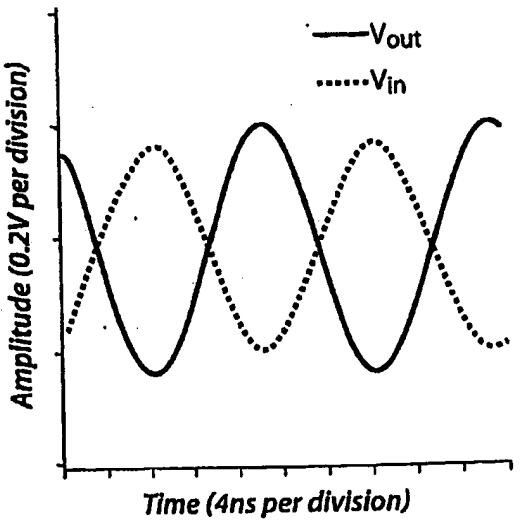


Fig. 12D

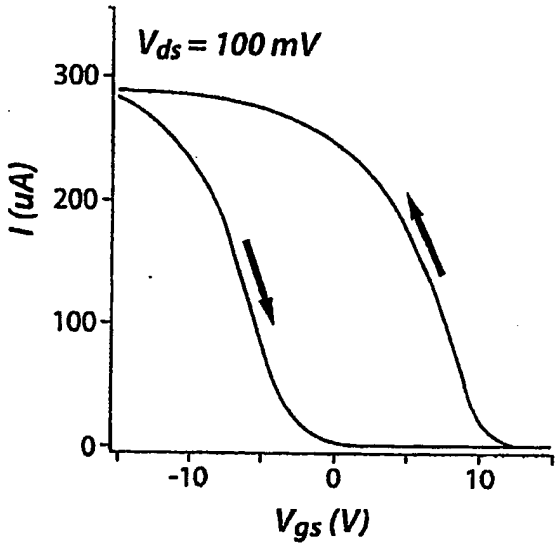


Fig. 13A

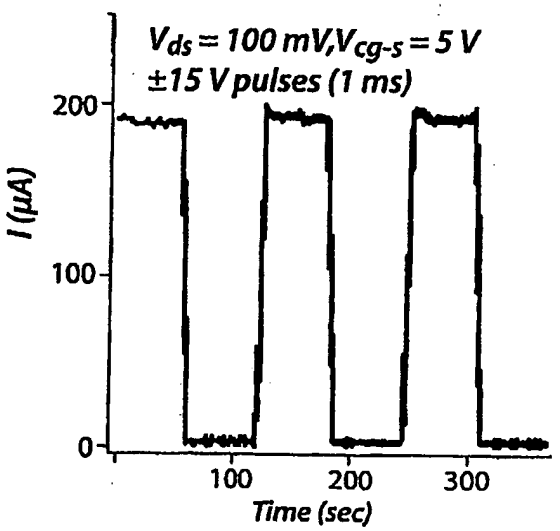


Fig. 13B

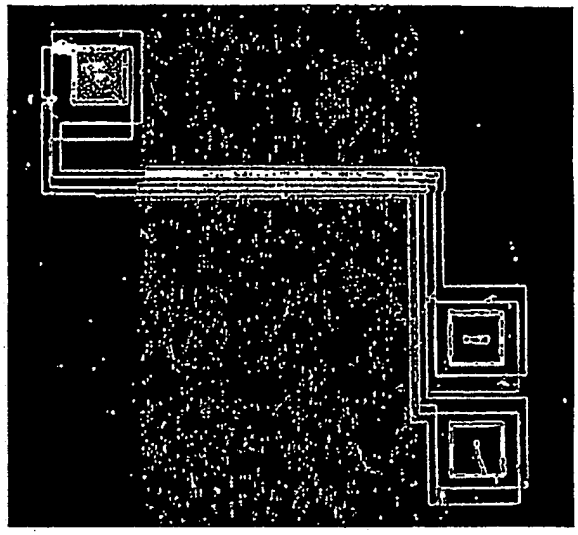


Fig.14A

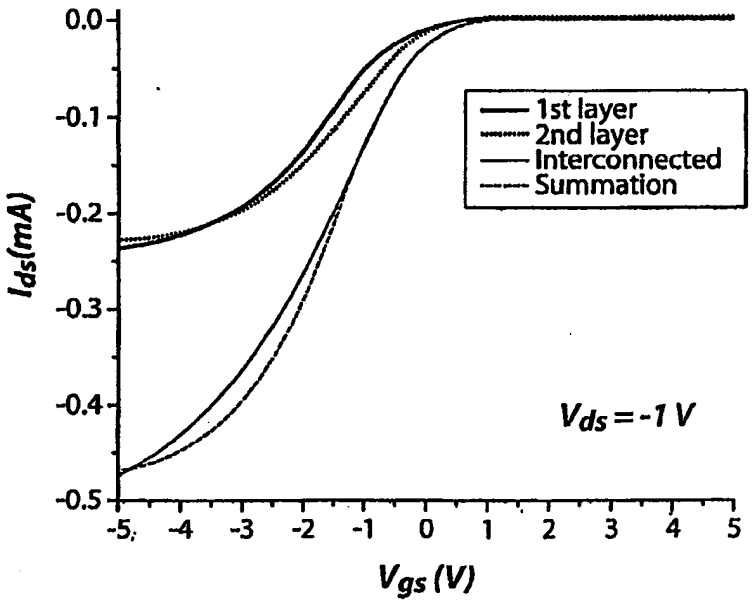


Fig.14B

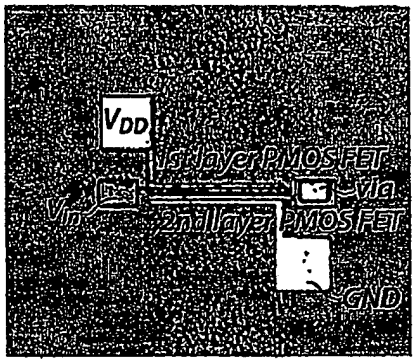


Fig. 15A

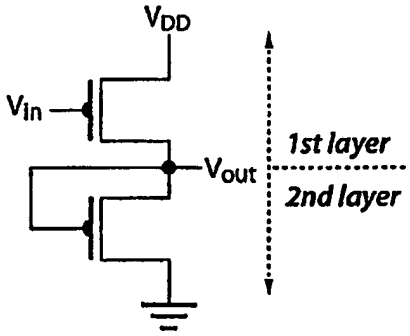


Fig. 15B

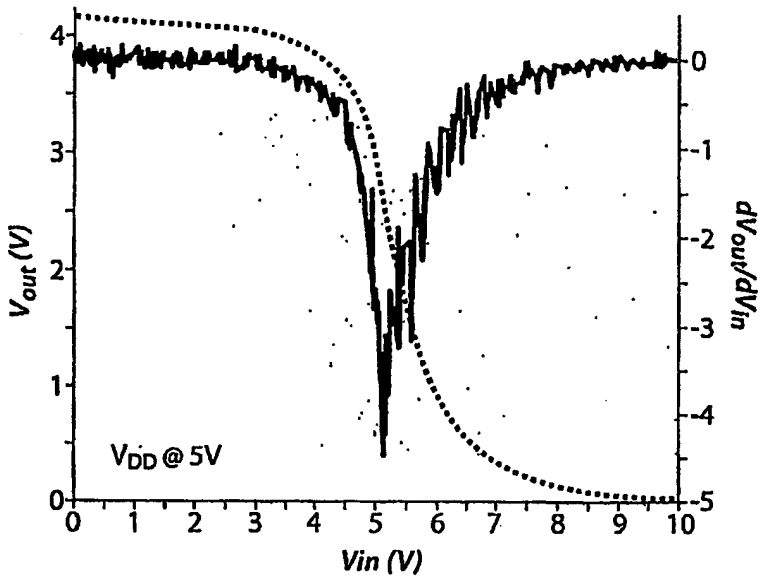


Fig. 15C

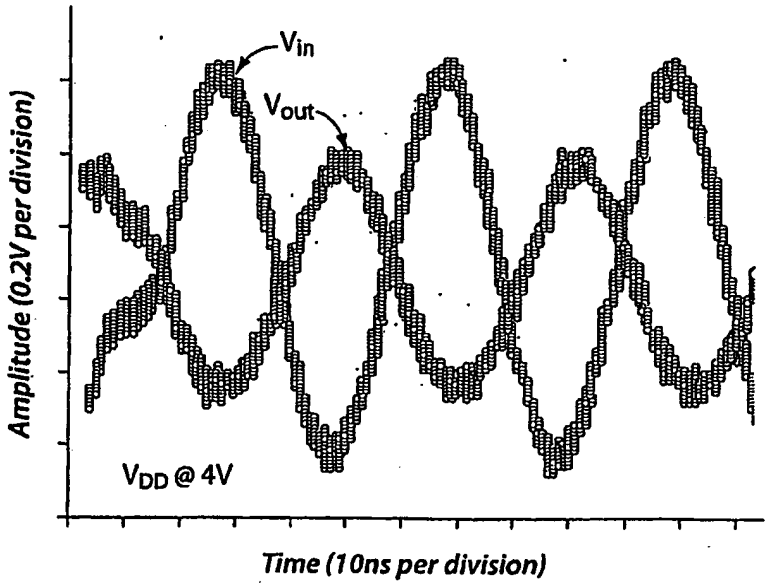


Fig. 15D

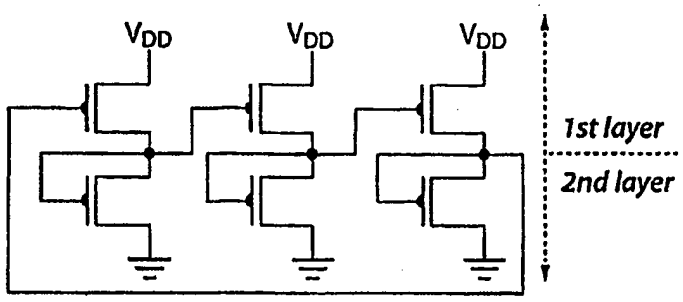


Fig. 16A

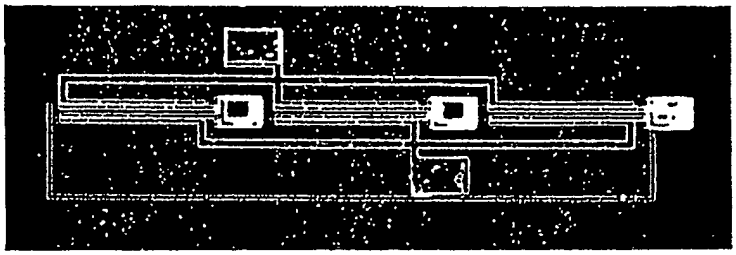


Fig. 16B

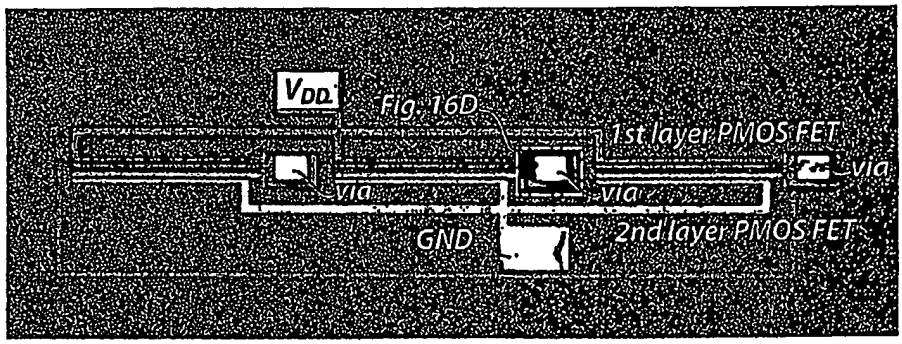


Fig. 16C

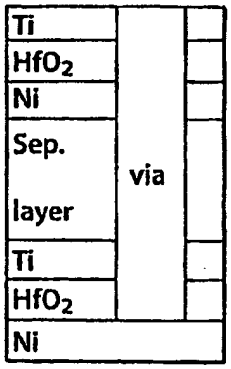


Fig. 16D

Cross section schematic diagram of via

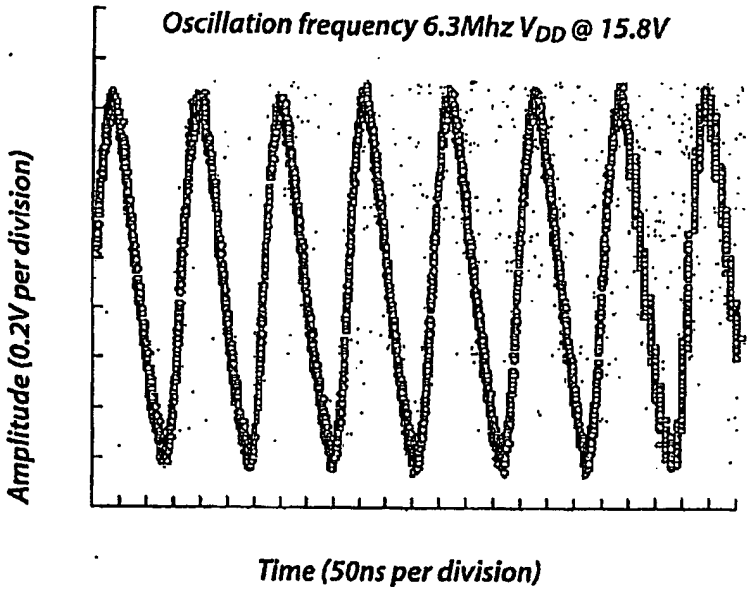


Fig. 16E

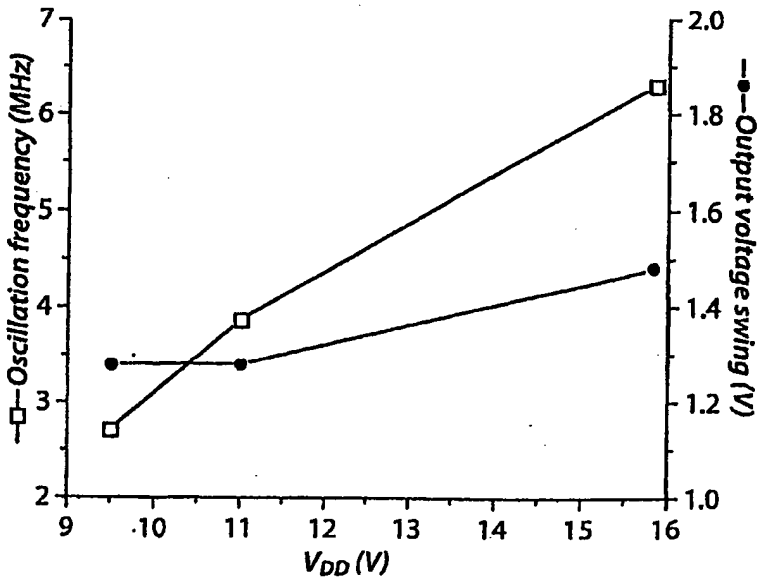


Fig. 16F

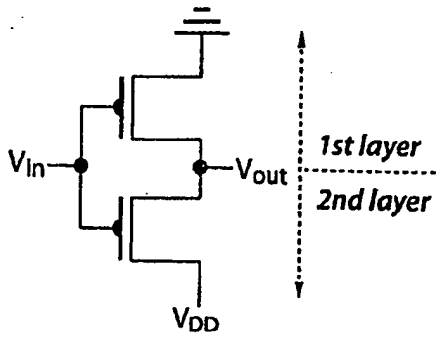


Fig. 17A

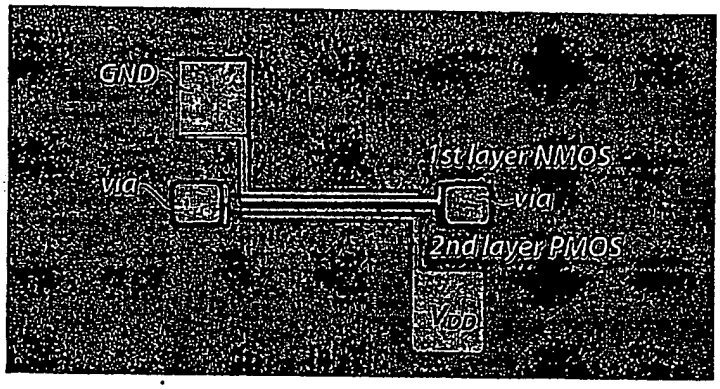


Fig. 17B

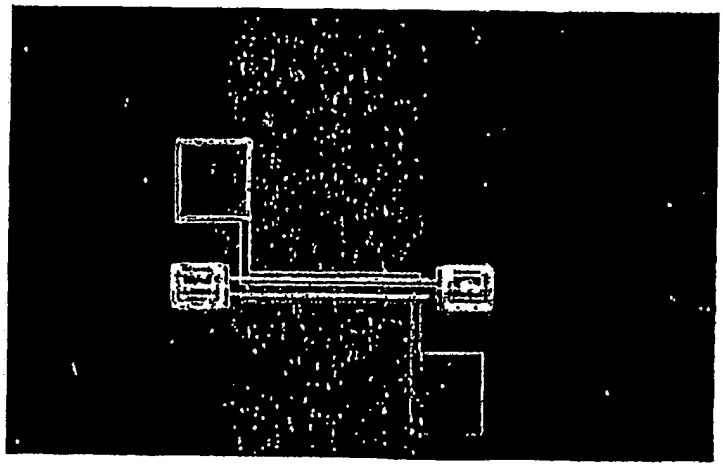


Fig. 17C

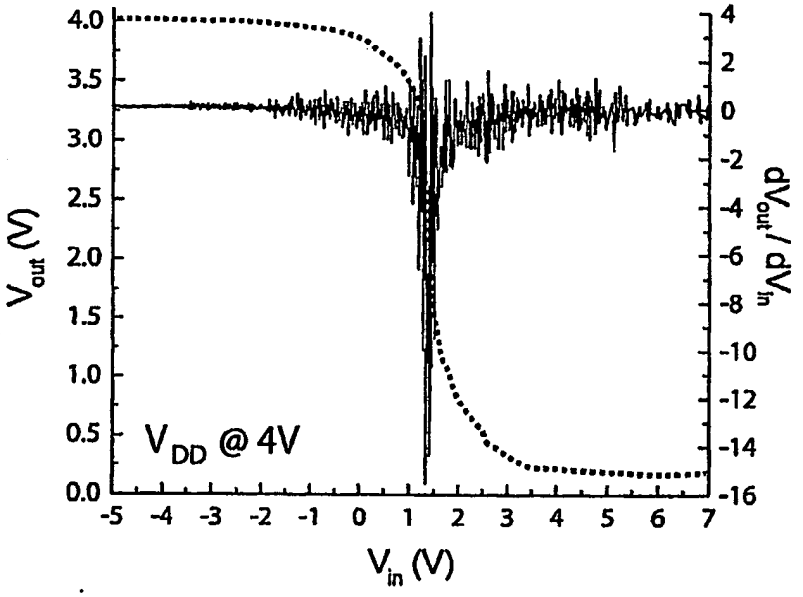


Fig. 17D

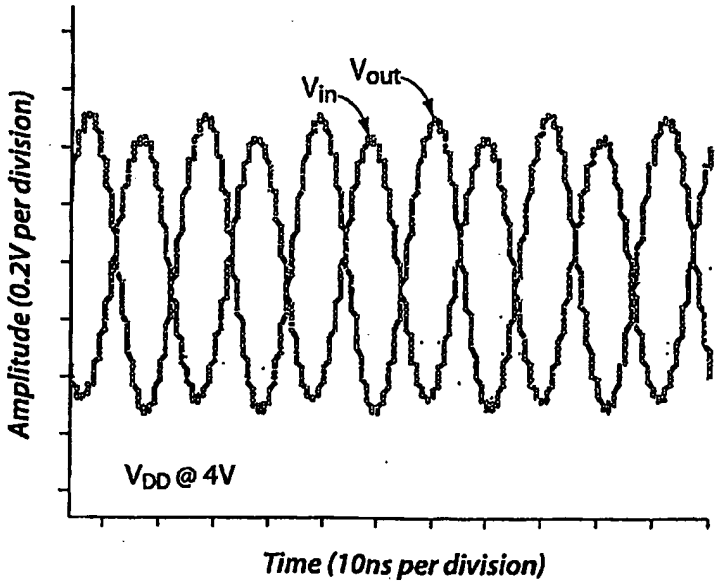


Fig. 17E

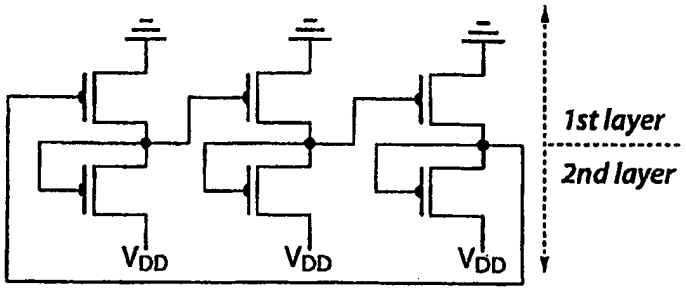


Fig. 18A

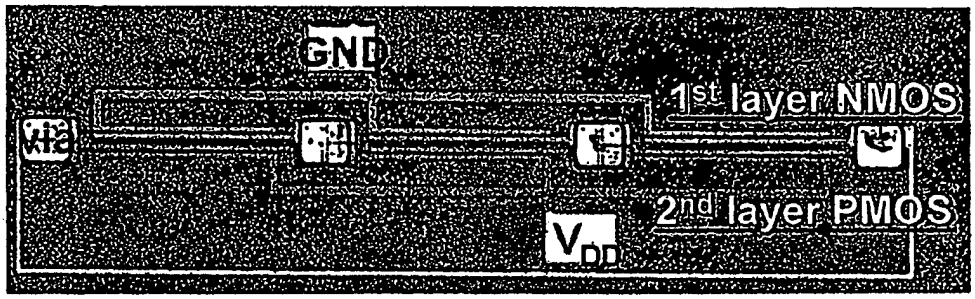


Fig. 18B

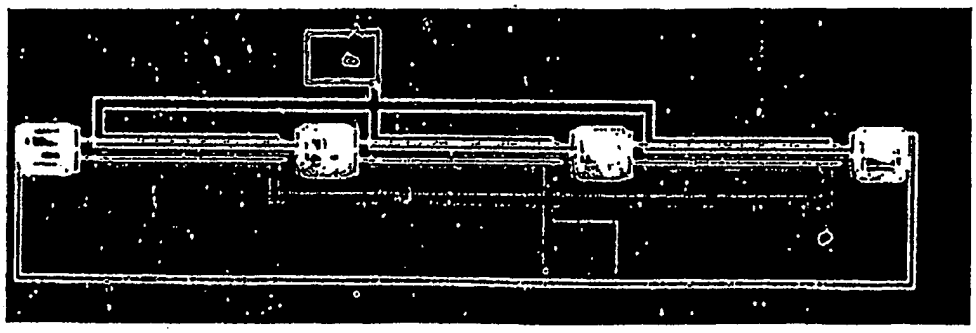


Fig. 18C

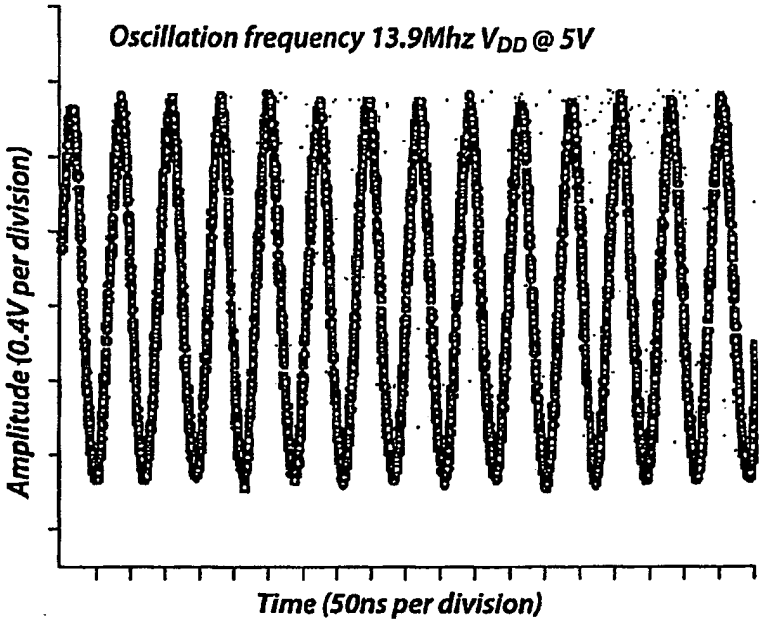

Oscillation frequency 13.9Mhz V_{DD} @ 5V
Amplitude (0.4V per division)
Time (50ns per division)

Fig. 18D